Himax Imaging, Ltd.

DATA SHEET

(DOC No. HM0435-DS)

HM0435

1/3.5″ 720 x 540 ▪ VGA 60FPS CMOS Image Sensor SoC

Version 14 April, 2023

Himax Imaging, Ltd.

HM0435 BrightSense™

1/3.5″ 720 x 540 ▪ VGA 60FPS CMOS Image Sensor SoC

Himax Imaging, Ltd.
http://www.himax.com.tw

April, 2023

Features

- 1/3.5" format sensor array with high performance 5.6µm x 5.6µm pixel that delivers 18.5V / lux–sec sensitivity
- Flexible sensor array window and pan readout with an additional ±40H and ±30V border pixels for lens alignment
- 60FPS progressive readout with support for multiple data formats including YUV, CCIR656, RGB565 / 555 / 444 and RAW
- On-chip Image Signal Processor with automatic exposure, flicker avoidance, gain, white balance, and image quality optimization control loop
- Integrated NTSC and PAL video encoder and driver with control over color burst parameters
- Overlay engine simultaneously displays two independent layers with 8 colors, 8 levels of transparencies, and separate offset control
- Support for SPI Flash memory with automatic initialization for overlay and sensor registers
- Support for SPI EEPROM memory with automatic initialization for sensor registers
- Dual sensor synchronization for frame start, exposure, gain and other video timing control
- Color and Monochrome options

Key Parameters

Sensor parameters	Value
Pixel Array **(Full / Active)**	728 x 548 / 720 x 540
Pixel Size	5.6µm x 5.6µm
Full Image Area	4032µm x 3024µm
Optical Format	5.04mm **(1/3.5″)**
Color Filter Array	Bayer, Monochrome
Scan Mode	Progressive
Shutter Type	Electronic Rolling Shutter
Frame Rate **(YUV / RAW)**	60FPS @ 54MHz / 27MHz
Frame Rate **(NTSC / PAL)**	50 / 60 fields/sec
S/N Ratio **(Max.)**	36.5 dB
DR **(1x)**	66.5 dB
Sensitivity **(Color)**	18.5 V / lux-sec
PRNU	< 1 %
CRA **(Max.)**	15.750º

General parameters	Value
Supply Voltage	AVDD: 3.0 – 3.6V **(3.3V Typ.)**
	DVDD: 1.35 – 1.65V **(1.5V Typ.)**
	IOVDD: 1.7 - 3.6V
Input Reference Clock	3 - 48MHz **(27MHz Typ.)**
Serial Interface **(I2C)**	2-Wire, 400kHz **(Max.)**
Serial Peripheral Interface	3.375MHz **(Typ.)**
Video Data Interface	10-bit parallel, CVBS
Output Format	8/10 bit Raw RGB, 8-bit YUV422, CCIR656, RGB565/555/444
Power Consumption	Active **(parallel@60FPS)** 182mW
	Active **(CVBS)** 254mW
	Power down 1µW

Order Information

Part no.	Color option	Operating / Storage temperature	Package
HM0435-AWB	RGB	-30 ºC to 85 ºC	CSP

Revision History

April, 2023

Version	Date	Description of changes
01	2013/10/31	New setup.
02	2013/12/02	1. Modify OTP2 power = 7.5V. 2. Modify Measurement results. 3. Modify IOVDD input range to 1.7V -3.6V.
03	2014/01/16	1. Modify pixel array size to 720 x 540. 2. Add 0.1µF between PWDN and IOVDD and 22kΩ between PWDN and IOGND in reference circuit. 3. Add Boot / IRS function control registers.
04	2014/02/24	1. Add register description. 2. The pin description of VQ: Power input for OTP1. **(Normal: 3.3V; Programming: 3.3V)** 3. Modify 4.16 Digital window. 4. Modify 4.17 Resolution and Scaling and windowing. 5. Modify 10.2 Frame rate control. 6. Modify 10.3 Exposure control. 7. Add 10.4 Flicker step. 8. Modify the capacitance value between PWDN and IOVDD from 0.1µF to 2.2µF in reference circuit. 9. Add a capacitor between IOVDD and DVDD in reference circuit.
05	2014/03/14	1. Modify 12.5 Serial bus characteristics.
06	2014/04/07	1. Remove “Preliminary” wording.
07	2014/06/26	1. Add temperature range of stable image. 2. Add test condition for power consumption measurement & modify power consumption results. 3. Correct typos.
08	2014/08/01	1. Add AWA/MWA package information. 2. Add power consumption in external LDO mode.
09	2014/11/19	1. Add 3.2 Analog window readout. 2. Add 10.5 Analog gain control. 3. Add 10.6 Digital gain control. 4. Add 14. Quantum Efficiency (QE). 5. Modify 6.1 Supply voltage sequence. 6. Remove APA/MPA order information. 7. Remove ‘LED control & IR-cut switch function’. 8. Correct typos.
10	2015/02/17	1. Remove PLCC package. 2. Add 4.24 Controllable black-white output function.
11	2015/04/10	1. Modify operating temperature range to -30ºC ~ 85ºC.
12	2015/10/13	1. Modify 12.5 Serial bus characteristics. 2. Modify optical format from 1/3” to 1/3.5”. 3. Modify Sensor CRA data.
13	2023/01/18	Page 2 1. Modify ‘Key Parameters’. 2. Modify ‘Order Information’. Page 51~76 3. Modify Ch. ‘11. Register Table’. Page 78 4. Modify Ch. ‘12.3. DC characteristics’. Page 85 5. Modify Ch. ‘14. Quantum Efficiency (QE)’.

Revision History

April, 2023

Version	Date	Description of changes
14	2023/04/13	Page 2 1. Modify ‘Features’. 2. Modify ‘Key Parameters’. Page 23 3. Modify Ch. ‘4.5. RAW noise filter’. Page 27 4. Modify Ch. ‘4.16. Digital window’. Page 54 5. Modify Ch. ‘11.2. Image operation registers [0x0010 – 0x001D]’. Page 59 6. Modify Ch. ‘11.7. Sensor control registers [0x007A – 0x007B]’. Page 60~62 7. Modify Ch. ‘11.8. ISP control registers [0x0100 – 0x0126]’.

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1. Package Information

1.1. Bare Die package

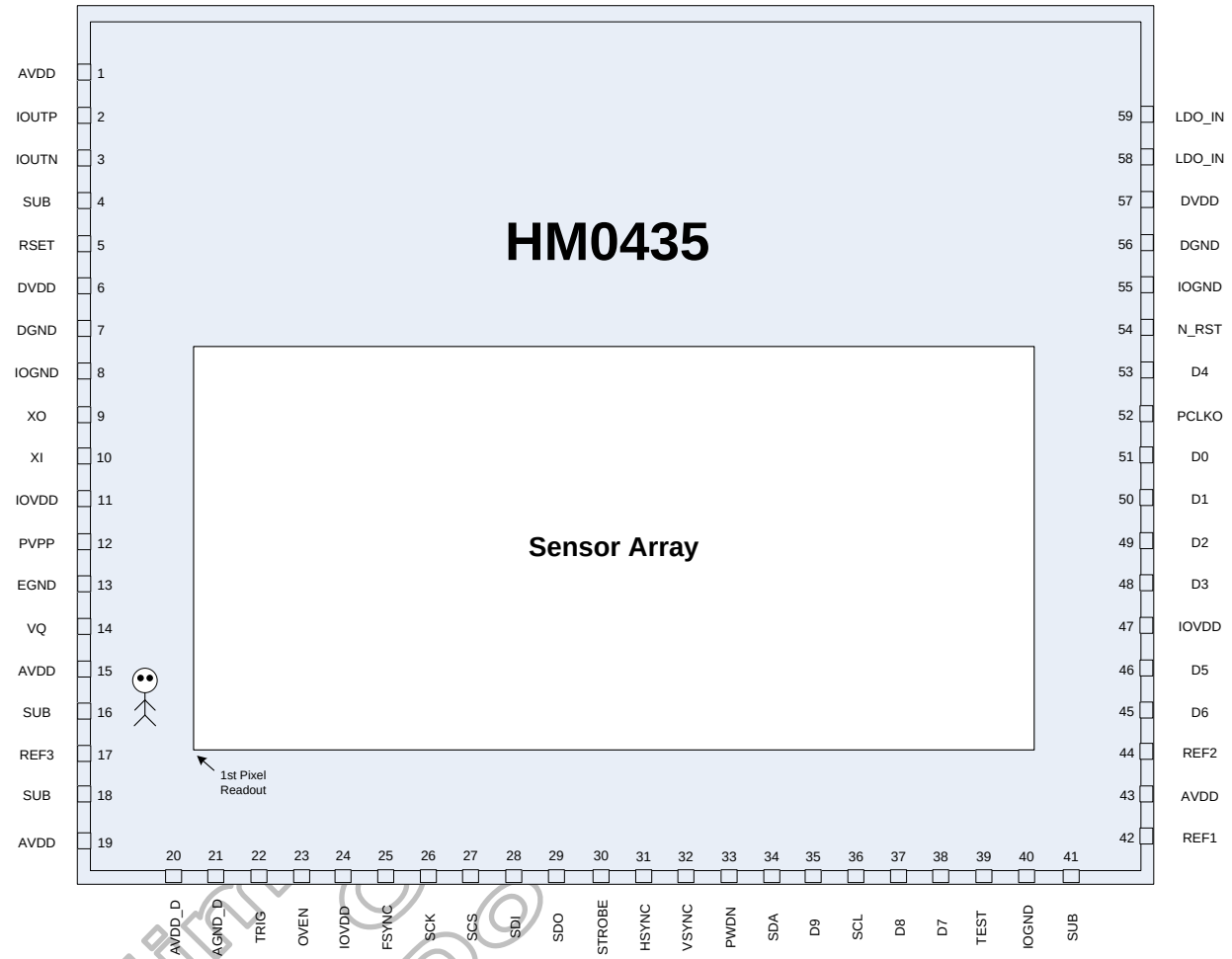


Figure 1.1: Bare Die pin diagram (Top view)

Pin no.	Pin name	Type	Internal Pull up / Pull down	Description
1	AVDD	POWER	N/A	Analog power. **(3.0V ~ 3.6V)**
2	IOUTP	OUTPUT	N/A	Video DAC output in single-ended mode. Positive video DAC output in differential mode.
3	IOUTN	OUTPUT	N/A	Negative video DAC output in differential mode.
4	SUB	GROUND	N/A	Pixel ground. **(Connect to ground plane)**
5	RSET	REFERENCE	N/A	Video DAC external reference resistor.
6	DVDD	POWER	N/A	Digital power.
7	DGND	GROUND	N/A	Digital ground.
8	IOGND	GROUND	N/A	IO ground.
9	XO	OUTPUT	N/A	If XI is connected to an oscillator, this pin should be left unconnected. Otherwise, this pin should be connected to the other pin of the crystal.
10	XI	INPUT	N/A	Master clock input: This pin can be connected to an oscillator **(In this case, XO is left unconnected)** or connected to a crystal.
11	IOVDD	POWER	N/A	I/O power. **(1.7V ~ 3.6V)**
12	PVPP	POWER	N/A	Power input for OTP2. **(Normal: floating, Programming: 7.5V)**
13	EGND	GROUND	N/A	Ground for OTP.
14	VQ	POWER	N/A	Power input for OTP1. **(Normal: 3.3V, Programming: 3.3V)**
15	AVDD	POWER	N/A	Analog power. **(3.0V ~ 3.6V)**
16	SUB	GROUND	N/A	Pixel ground. **(Connect to ground plane)**
17	REF3	REFERENCE	N/A	Voltage reference.
18	SUB	GROUND	N/A	Pixel ground. **(Connect to ground plane)**
19	AVDD	POWER	N/A	Analog power. **(3.0V ~ 3.6V)**
20	AVDD_D	POWER	N/A	Analog column power.
21	AGND_D	GROUND	N/A	Analog ground.
22	TRIG	I/O	Pull down	Output synchronous trigger signal for 3D-Sync.
23	OVEN	INPUT	Pull up	Overlay enable. If input level is low, tri-state the SPI bus.
24	IOVDD	POWER	N/A	I/O power. **(1.7V ~ 3.6V)**
25	FSYNC	I/O	Pull down	Input signal for 3D-Sync. LED_IRS: IRSI, illumination sensor input.
26	SCK	OUTPUT	N/A	Clock output. **(SPI: Serial Peripheral Interface)**
27	SCS	OUTPUT	N/A	Chip select. **(SPI: Serial Peripheral Interface)**
28	SDI	INPUT	Pull down	Data input. **(SPI: Serial Peripheral Interface)**
29	SDO	I/O	Pull down	Data output. **(SPI: Serial Peripheral Interface)**
30	STROBE	OUTPUT	N/A	LED strobe. LED_IRS: LED control.
31	HSYNC	I/O	Pull down	Horizontal sync output. Boot strap pin: FLK[0]
32	VSYNC	I/O	Pull down	Vertical sync output. Boot strap pin: FLK[1]
33	PWDN	INPUT	Pull down	Reset and power down control pin. **(Active high)** L: Normal. H: Power saving mode.
34	SDA	I/O	N/A	Data bus. **(Open Drain) (I2C-bus)**
35	D9	I/O	Pull down	Video data output. Boot strap pin: bw.
36	SCL	INPUT	N/A	Clock input. **(I2C-bus)**
37	D8	I/O	Pull up	Video data output. Boot strap pin: boot.
38	D7	I/O	Pull down	Video data output. Boot strap pin: VFlip.
39	TEST	INPUT	Pull down	Enable test mode for CP.
40	IOGND	GROUND	N/A	IO ground.

Pin no.	Pin name	Type	Internal Pull up / Pull down	Description
41	SUB	GROUND	N/A	Pixel ground. **(Connect to ground plane)**
42	REF1	REFERENCE	N/A	Voltage reference.
43	AVDD	POWER	N/A	Analog power. **(3.0V ~ 3.6V)**
44	REF2	REFERENCE	N/A	Voltage reference.
45	D6	I/O	Pull down	Video data output. Boot strap pin: HMirror.
46	D5	I/O	Pull down	Video data output. Boot strap pin: i2cid. L: Addr =0x24. **(7-bit)** H: Addr =0x34. **(7-bit)**
47	IOVDD	POWER	N/A	I/O power. **(1.7V ~ 3.6V)**
48	D3	I/O	Pull down	Video data output. Boot strap pin: DF[2].
49	D2	I/O	Pull down	Video data output. Boot strap pin: DF[1].
50	D1	I/O	Pull down	Video data output. Boot strap pin: DF[0]. LED_IRS: IRS1, IR cut switch control.
51	D0	I/O	Pull up	Video data output. Boot strap pin: SPI device selection. L: Flash. H: EEPROM. LED_IRS: IRS0, IR cut switch control.
52	PCLKO	OUTPUT	N/A	Pixel clock output.
53	D4	I/O	Pull down	Video data output. Boot strap pin: DF[3].
54	N_RST	INPUT	Pull up	Chip reset. **(Active low)**
55	IOGND	GROUND	N/A	IO ground.
56	DGND	GROUND	N/A	Digital ground.
57	DVDD	POWER	N/A	Digital power.
58	LDO_IN	POWER	N/A	If using bypass mode, LDO:1.5V. Otherwise LDO: 1.8V ~ 3.6V.
59	LDO_IN	POWER	N/A	If using bypass mode, LDO:1.5V. Otherwise LDO: 1.8V ~ 3.6V.

Table 1.1: Bare Die pin description

1.2. CSP package

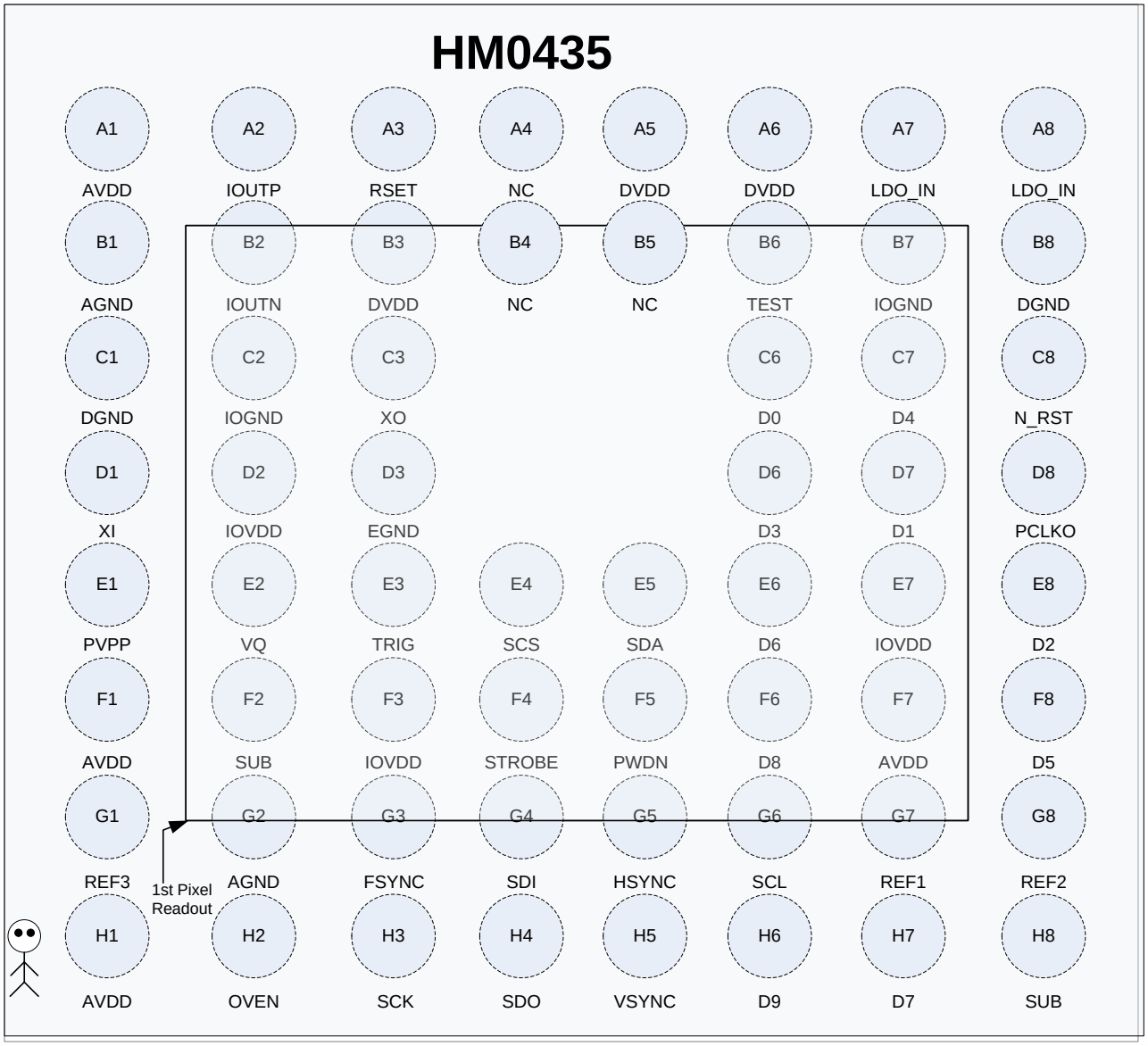


Figure 1.2: CSP pin diagram (Top view)

Pin no.	Pin name	Type	Internal Pull up / Pull down	Description
A1	AVDD	POWER	N/A	Analog power. **(3.0V ~ 3.6V)**
A2	IOUTP	OUTPUT	N/A	Video DAC output in single-ended mode. Positive video DAC output in differential mode.
A3	RSET	REFERENCE	N/A	Video DAC external reference resistor.
A4	NC	-	N/A	-
A5	DVDD	POWER	N/A	Digital power.
A6	DVDD	POWER	N/A	Digital power.
A7	LDO_IN	POWER	N/A	If using bypass mode: LDO: 1.5V, Otherwise LDO: 1.8V ~ 3.6V.
A8	LDO_IN	POWER	N/A	If using bypass mode: LDO: 1.5V, Otherwise LDO: 1.8V ~ 3.6V.
B1	AGND	GROUND	N/A	Analog ground.
B2	IOUTN	OUTPUT	N/A	Negative video DAC output in differential mode.
B3	DVDD	POWER	N/A	Digital power.
B4	NC	-	N/A	-
B5	NC	-	N/A	-
B6	TEST	INPUT	Pull down	Enable test mode for CP.
B7	IOGND	GROUND	N/A	IO ground.
B8	DGND	GROUND	N/A	Digital ground.
C1	DGND	GROUND	N/A	Digital ground.
C2	IOGND	GROUND	N/A	IO ground.
C3	XO	OUTPUT	N/A	If XI is connected to an oscillator, this pin should be left unconnected. Otherwise, this pin should be connected to the other pin of the crystal.
C6	D0	I/O	Pull up	Video data output. Boot strap pin: SPI device selection, L: Flash, H: EEPROM. LED_IRS: IRS0, IR cut switch control.
C7	D4	I/O	Pull down	Video data output. Boot strap pin: DF[3].
C8	N_RST	INPUT	Pull up	Chip reset. **(Active low)**
D1	XI	INPUT	N/A	Master clock input: This pin can be connected to an oscillator **(In this case, XO is left unconnected)** or connected to a crystal.
D2	IOVDD	POWER	N/A	I/O power. **(1.7V ~ 3.6V)**
D3	EGND	GROUND	N/A	Ground for OTP.
D6	D3	I/O	Pull down	Video data output. Boot strap pin: DF[2].
D7	D1	I/O	Pull down	Video data output. Boot strap pin: DF[0] LED_IRS: IRS1, IR cut switch control.
D8	PCLKO	OUTPUT	N/A	Pixel clock output.
E1	PVPP	POWER	N/A	Power input for OTP2. **(Normal: floating, Programming: 7.5V)**
E2	VQ	POWER	N/A	Power input for OTP1. **(Normal: 3.3V, Programming: 3.3V)**
E3	TRIG	I/O	Pull down	Output synchronous trigger signal for 3D-Sync.
E4	SCS	OUTPUT	N/A	Chip select. **(SPI: Serial Peripheral Interface)**
E5	SDA	I/O	N/A	Data bus. **(Open Drain) (I2C-bus)**
E6	D6	I/O	Pull down	Video data output. Boot strap pin: HMirror.
E7	IOVDD	POWER	N/A	I/O power. **(1.7V ~ 3.6V)**
E8	D2	I/O	Pull down	Video data output. Boot strap pin: DF[1].
F1	AVDD	POWER	N/A	Analog power. **(3.0V ~ 3.6V)**
F2	SUB	GROUND	N/A	Pixel ground. **(Connect to ground plane)**

Pin no.	Pin name	Type	Internal Pull up / Pull down	Description
F3	IOVDD	POWER	N/A	I/O power. **(1.7V ~ 3.6V)**
F4	STROBE	OUTPUT	N/A	LED strobe. LED_IRS: LED control.
F5	PWDN	INPUT	Pull down	Reset and power down control pin. **(Active high)** L: Normal, H: Power saving mode.
F6	D8	I/O	Pull up	Video data output. Boot strap pin: boot.
F7	AVDD	POWER	N/A	Analog power. **(3.0V ~ 3.6V)**
F8	D5	I/O	Pull down	Video data output. Boot strap pin: i2cid, L: Addr =0x24. **(7-bit)** H: Addr =0x34. **(7-bit)**
G1	REF3	REFERENCE	N/A	Voltage reference.
G2	AGND	GROUND	N/A	Analog ground.
G3	FSYNC	I/O	Pull down	Input signal for 3D-Sync. LED_IRS: IRSI, illumination sensor input.
G4	SDI	INPUT	Pull down	Data input. **(SPI: Serial Peripheral Interface)**
G5	HSYNC	I/O	Pull down	Horizontal sync output. Boot strap pin: FLK[0].
G6	SCL	INPUT	N/A	Clock input. **(I2C-bus)**
G7	REF1	REFERENCE	N/A	Voltage reference.
G8	REF2	REFERENCE	N/A	Voltage reference.
H1	AVDD	POWER	N/A	Analog power **(3.0V ~ 3.6V)**
H2	OVEN	INPUT	Pull up	Overlay enable. If input level is low, tri-state the SPI bus.
H3	SCK	OUTPUT	N/A	Clock output. **(SPI: Serial Peripheral Interface)**
H4	SDO	I/O	Pull down	Data output. **(SPI: Serial Peripheral Interface)**
H5	VSYNC	I/O	Pull down	Vertical sync output. Boot strap pin: FLK[1]
H6	D9	I/O	Pull down	Video data output. Boot strap pin: bw.
H7	D7	I/O	Pull down	Video data output. Boot strap pin: VFlip.
H8	SUB	GROUND	N/A	Pixel ground. **(Connect to ground plane)**

Table 1.2: CSP pin description

2. Sensor Overview

The HM0435 is a standard resolution VGA image sensor SOC that delivers excellent low light sensitivity and noise performance in a compact 30 mm^2 chip scale package. The sensor provides 640 x 480 active pixels that can be panned across an additional 80 horizontal pixels and 60 vertical pixels to compensate for camera lens alignment tolerance.

The HM0435 features Himax Imaging's ClearView™ ISP that enhances the sharpness and clarity of the image based on the optical properties of the lens. The on-chip automatic exposure, gain, white balance and ISP parameters quickly adapt the sensor across a broad range of lighting conditions.

The HM0435 supports multiple sensor initialization options using internal or external memory. The sensor offers a high level of integration including voltage regulators, temperature sensor, crystal oscillator, fast locking clock generator, and analog video encoder with current driver. The HM0435 enables the design of compact full-featured camera system for a wide variety of camera applications.

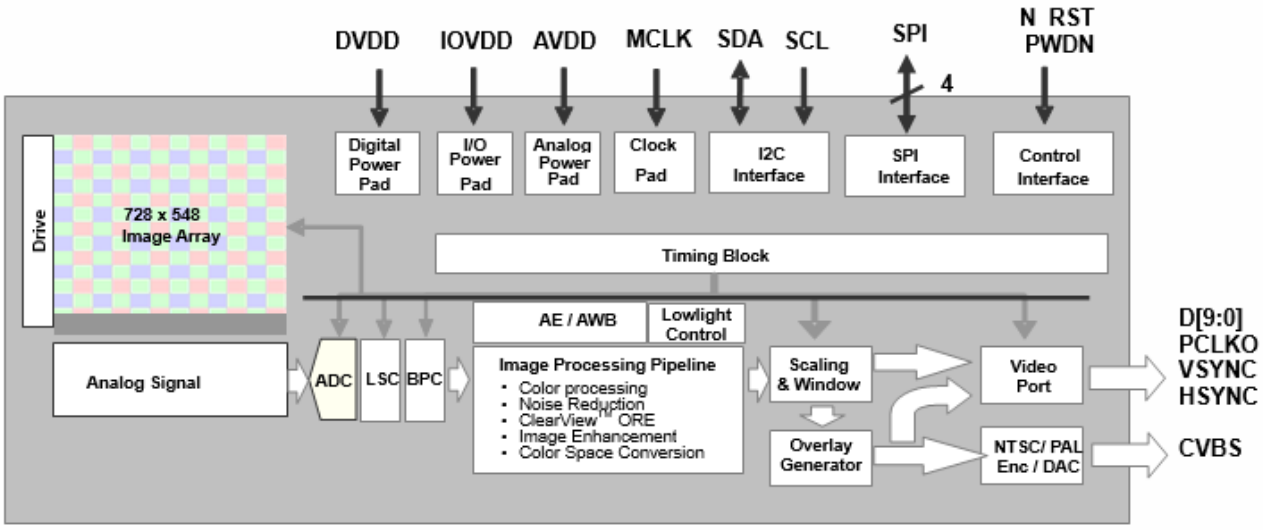


Figure 2.1: HM0435 block diagram

3. Sensor Core and Function Description

3.1. Sensor array

The HM0435 has a full active pixel array of 728 x 548. The even numbered rows contain the Blue **(B)** and Green **(G_1)** pixel, and the odd numbered row contains the Red **(R)** and Green **(G_2)** pixels. The even numbered columns contain the Green **(G_2)** and Blue **(B)** pixels, and the odd column contains the Red **(R)** and Green **(G_1)** pixels. There are 8 black rows used by the sensor for black level calibration. Programmable horizontal and vertical blanking time adjusts the line width and frame height, respectively.

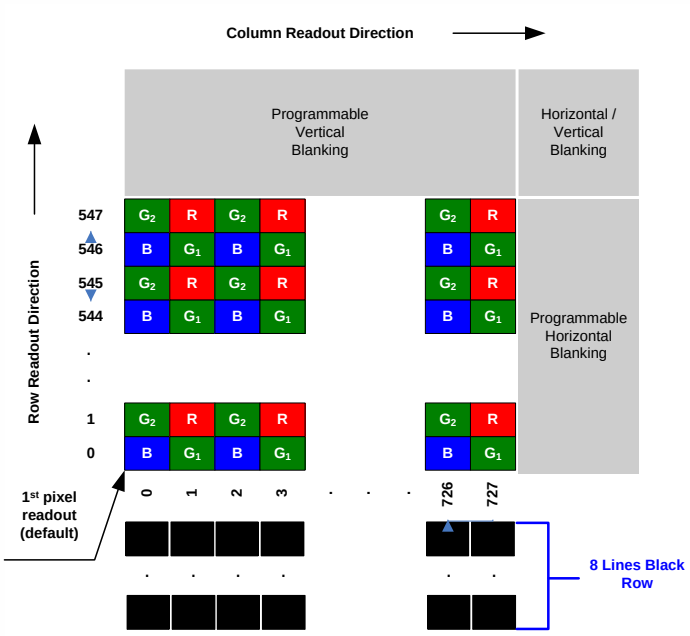


Figure 3.1: Full resolution pixel readout

3.2. Analog window readout

Analog window selects the coordinates of the pixel array readout. The frame timing will be changed according to the settings.

- Setting **RDCFG[3:2]**=0x00, the full pixel array **(728x548)** will output.
- Arbitrary window readout is enabled by setting **RDCFG[3:2]**=0x01.
- Programming window size by specifying x **(Horizontal)** and y **(Vertical)** starting and ending position
  - X Start: **AnaWinHStart_1[1:0], AnaWinHStart_0[7:0]**
  - Y Start: **AnaWinVStart_1[1:0], AnaWinVStart_0[7:0]**
  - X End: **AnaWinHEnd_1[1:0], AnaWinHEnd_0[7:0]**
  - Y End: **AnaWinVEnd_1[1:0], AnaWinVEnd_0[7:0]**
- For color version, the X Start / Y Start should be set to an even number of pixels to maintain the color order.

Address	Register ID	Value
0x50	AnaWinVStart_1	0x00
0x51	AnaWinVStart_0	0x1E
0x52	AnaWinVEnd_1	0x02
0x53	AnaWinVEnd_0	0x05
0x54	AnaWinHStart_1	0x00
0x55	AnaWinHStart_0	0x28
0x56	AnaWinHEnd_1	0x02
0x57	AnaWinHEnd_0	0xAF

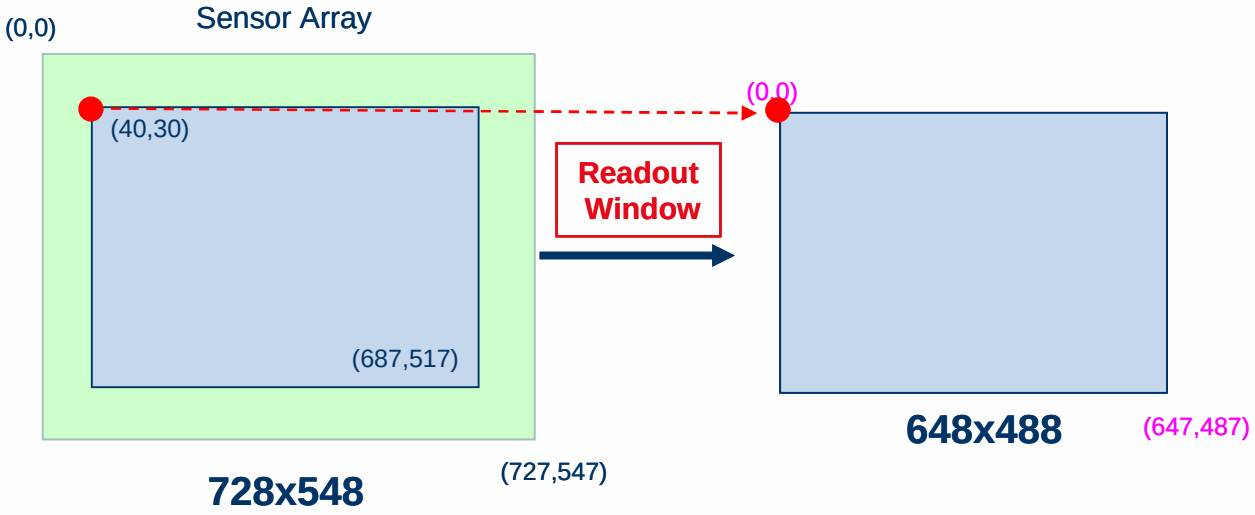
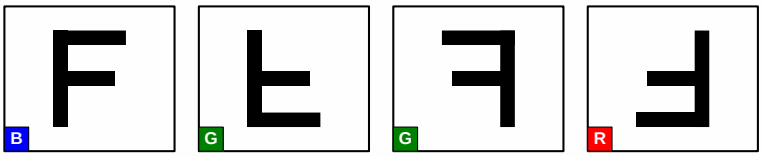


Figure 3.2: Sample readout setting for NTSC0 analog window located in the center of the frame

3.3. Horizontal and Vertical mirror

The sensor readout can be mirrored in the vertical and / or horizontal direction.

- In vertical mirror **(flip)** readout mode. the rows are readout in reverse order, which will result in the appearance of the image being flipped upside down.
- In horizontal mirror readout mode, the columns are readout in reverse order, which will result in the appearance of the image being flipped along the vertical axis.
- Horizontal and vertical mirror readout can be used in all readout modes.



Default
RDCFG[1:0] = 00

Vertical Mirror
RDCFG[1:0] = 01

Horizontal Mirror
RDCFG[1:0] = 10

V & H Mirror
RDCFG[1:0] = 11

Figure 3.3: Horizontal and Vertical mirror readout modes

4. Digital Functional Description

Image processing and automatic control loop functions are performed by the Image Processor Pipeline **(IPP)**. The IPP can be configured by the host through the serial register interface. The IPP includes Automatic Exposure function which controls dynamic range, exposure, and gamma, as well as blending parameters.

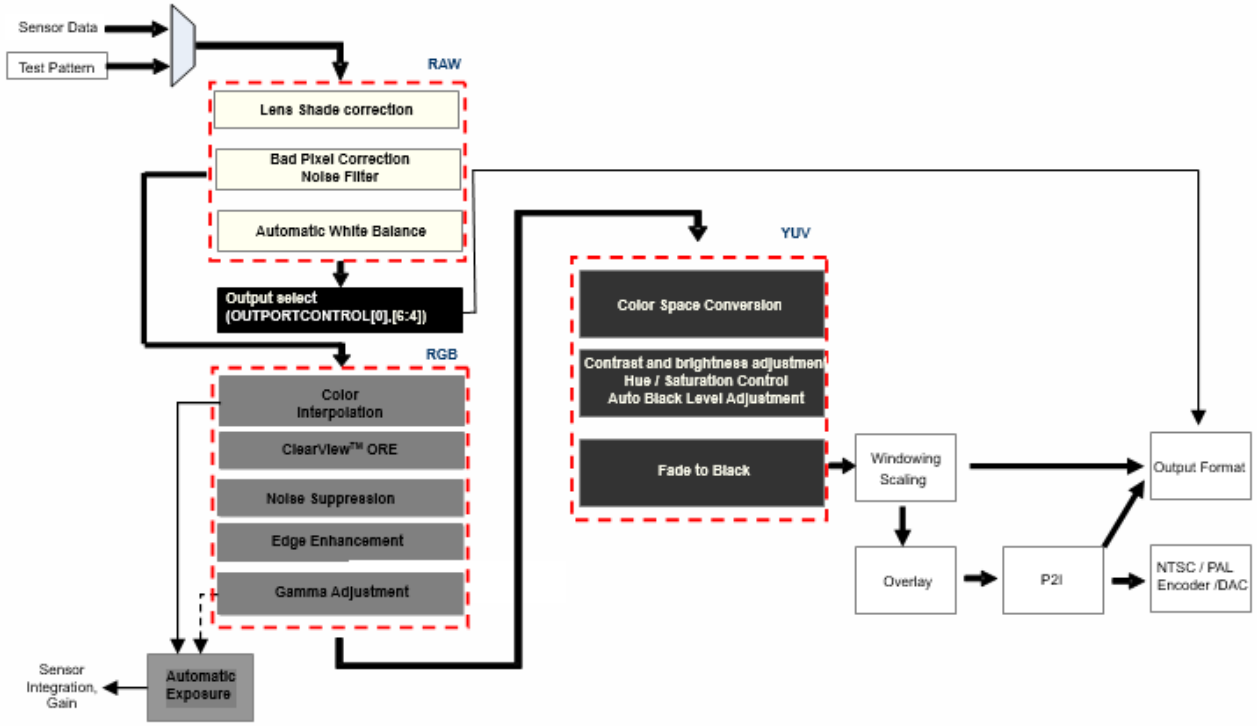


Figure 4.1: IPP signal chain

4.1. Test pattern

On-chip test patterns can be enabled by setting bit **CKMUL[7]** and selecting one of sixteen available patterns using **CKMUL[3:0]** register. The test pattern bypasses the sensor core and analog signal chain and can be used to test sensor communication, digital pipeline and video port.

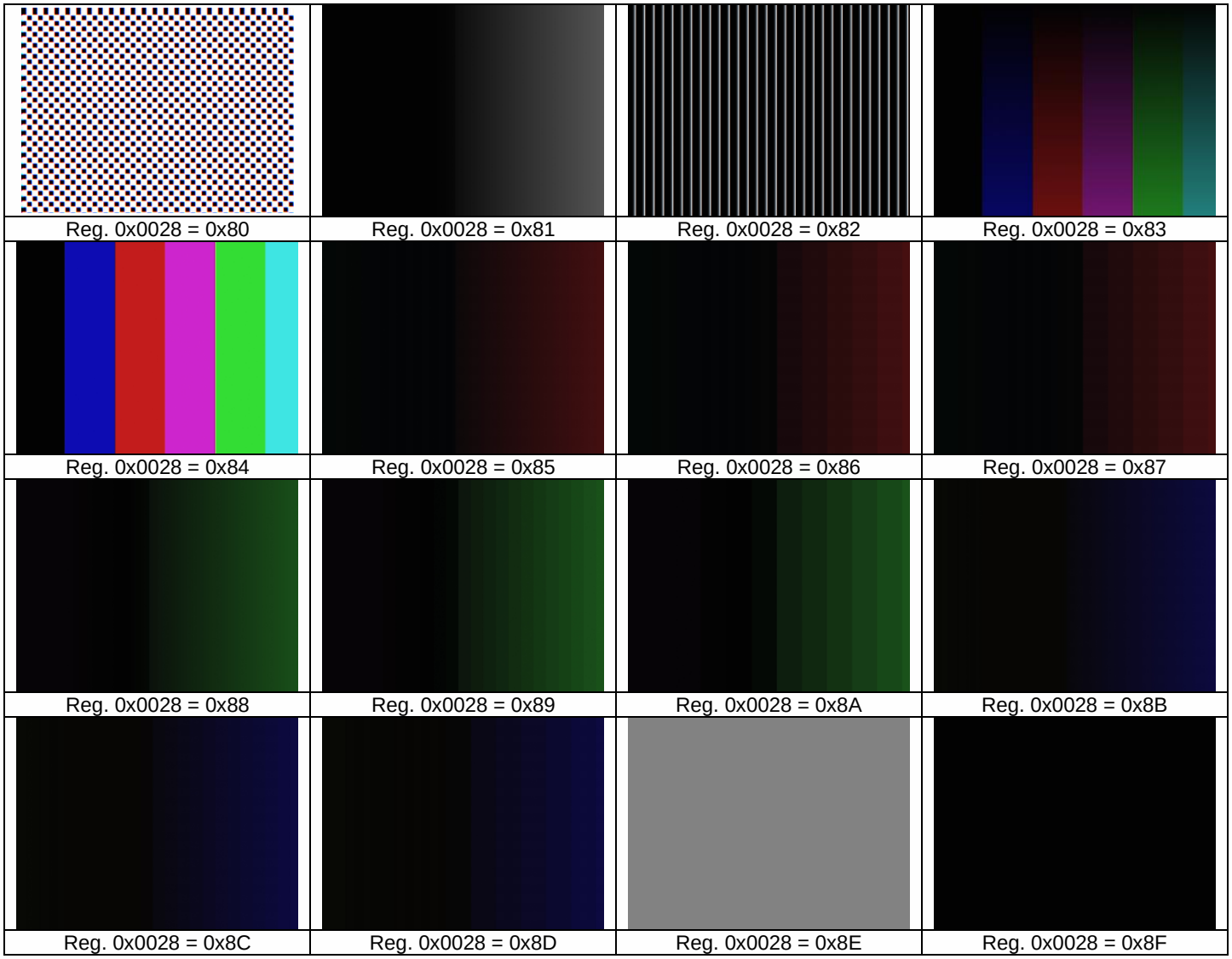


Figure 4.2: Test image patterns

Additional EIA color bars **(NTSC)** test pattern and EBU color bars **(PAL)** test pattern are provided to support verification and tuning of color levels.

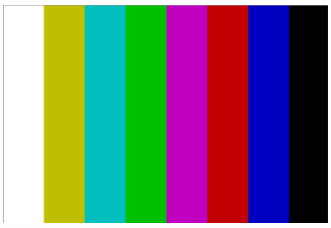


Figure 4.3: EIA/EBU color bars

	White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
Y	180	162	131	112	84	65	35	16
Cb	128	44	156	72	184	100	212	128
Cr	128	142	44	58	198	212	114	128

Table 4.1: EIA color bars (NTSC)

	White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
Y	235	162	131	112	84	65	35	16
Cb	128	44	156	72	184	100	212	128
Cr	128	142	44	58	198	212	114	128

Table 4.2: EBU color bars (PAL)

4.2. Black level calibration

The shielded pixels within the sensor array are continuously sampled and on-chip black level control loop automatically applies an offset so that the average black level of each frame tracks the programmed target mean values.

4.3. Lens Shading Correction (LSC)

The lens and module assembly can reduce the illumination and induce visible hue shift at the peripheries of the sensor array. To minimize this effect, the Lens Shading Correction **(LSC)** circuit compensates this effect by applying a multi-channel polynomial correction factor to the pixel data as a function of distance from the lens center. Programmable coefficients adjust the behavior of the compensation curve and the center offset. Additional strength adjustment scales the compensation curve from 0 to full compensation in step sizes of 1/16.

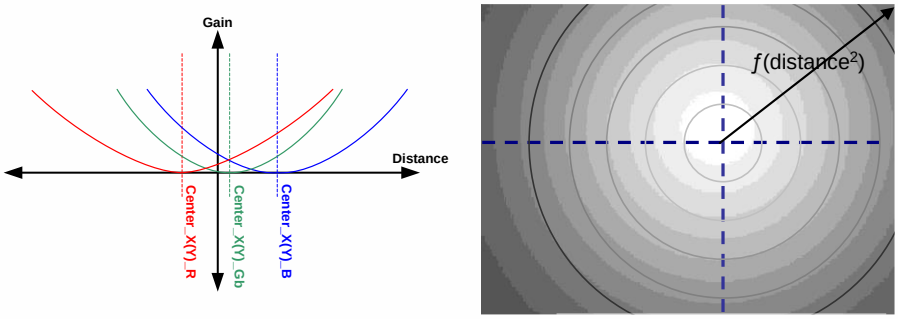


Figure 4.4: Lens Shading Correction (LSC)

4.4. Bad Pixel Correction (BPC)

On-the-fly bad pixel correction masks hot and cold pixel defects by comparing each pixel to BPC threshold value derived from a region of neighboring same-color pixels. The BPC algorithm detects presence of edge within the neighboring pixel window and filters out the detected edge pixels from the threshold computation to minimize false detection.

4.5. RAW noise filter

The noise filter adaptively suppresses temporal noise in flat areas of the scene. The strength of the temporal noise filter can be set through the **Denoise_iStrength[5:0]** register.

4.6. Color interpolation

Each 10-bit raw pixel data is converted to RGB value using an edge-sensitive color interpolation algorithm. The interpolation utilizes a weighted combination of neighboring pixels to preserve distinct edges and minimize color artifacts.

4.7. Color correction

The color correction multiplies the interpolated RGB value a by programmable 3x3 matrix to map the color response of the sensor to a desired target. The matrix values are determined based on the spectral response and the cross talk characteristics of the sensor. A mode is provided to interpolate the effective correction matrix between two programmed matrices based on the spectral response of the sensor to different light color temperatures as described in the Dynamic Parameter Scaling section.

4.8. Gamma correction

The gamma curve is comprised of an 8-bit piece-wise linear curve, which is applied equally to the R, G and B color channel. The input data points are as follows: 4, 8, 16, 32, 40, 48, 56, 64, 72, 80, 96, 112, 144, 176, 208 and 255. The gamma correction can be bypassed through the serial register by setting register bit **ISPCtrl_byte1[2]** to 0.

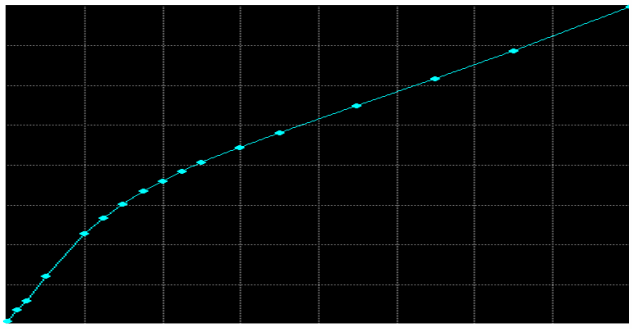
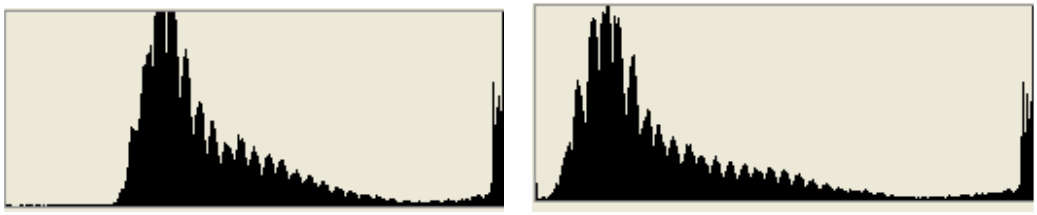


Figure 4.5: Piece-wise gamma curve

4.9. Automatic Black Level Adjustment (ABLA)

In order to dynamically enhance the contrast of each scene, the ABLA analyzes the scene and redistributes the luminance channel to fully utilize the low tone.



Initial scene histogram Post-Black Level adjustment

Figure 4.6: Automatic Black Level Adjustment (ABLA) example

4.10. Saturation and Hue adjustment

Color saturation adjustment provides additional control for color preference and can be adjusted by register **SatB[7:0]**. The hue of a color can be manipulated by rotating the hue about the gray vector using the **HueSIN[7:0]** and **HueCOS[7:0]** registers.

4.11. Contrast and Brightness adjustment

Contrast adjustment consists of a 4 segment piecewise linear curve which provides flexibility to program different contrast schemes from the basic linear contrast to segment s-curve contrast. The contrast segments **(M, N, P)** are controlled by programming the slopes and the center point.

Brightness adjustment adds or subtracts an offset of the luminance channel. The Brightness can be adjusted by setting register **BN_BRIGHTNESS[7:0]**.

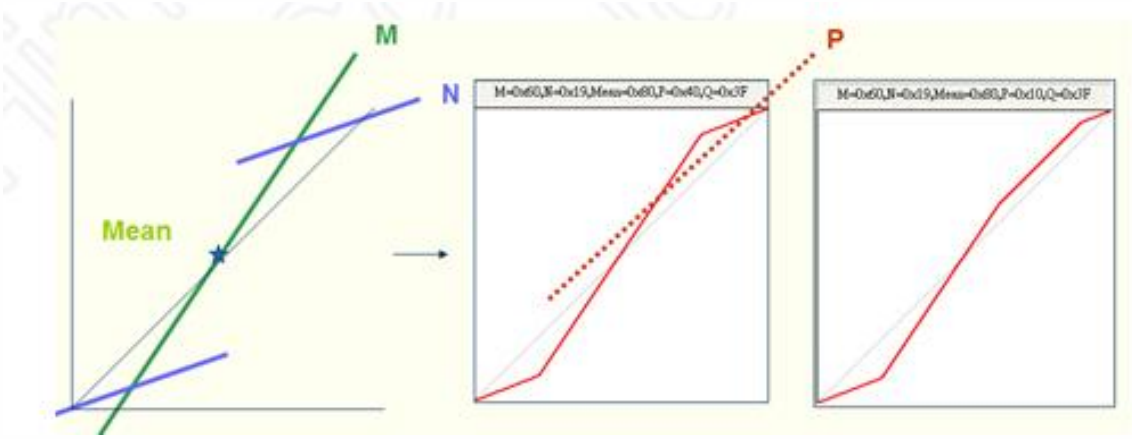


Figure 4.7: Contrast curve example

4.12. YCbCr noise reduction

Noise reduction is applied separately to the luminance **(Y)** channel and chrominance **(CbCr)** channel. The luminance noise reduction algorithm is edge-sensitive with configurable thresholds to balance the integrity of the edge with noise reduction.

4.13. Edge enhancement

A 2-dimensional sharpening filter can be applied to the luminance component of the image. The strength of enhancement is set by the **EE_SHARP_EDGE[7:0]** register.

4.14. Automatic lowlight control

Several image pipeline parameters can be dynamically adjusted based on the brightness of the scene to improve image quality. The range of the individual parameters defines the maximum and minimum magnitude or threshold for the specific image pipeline parameter. A programmable curve, defined by registers **Alpha1_Coef[7:0]** to **Alpha8_Coef[7:0]**, applies the scaling factor to determine the actual setting of the specific parameter.

4.15. Overlay engine

The overlay engine utilizes SPI interface to load overlay content from external flash with the following features:

- Up to two overlay layers may be blended simultaneously with individually programmable line height, width, x & y coordinate
- Up to 256 overlay images could be stored in the external flash memory for manually fast overlay switch
- Each overlay image has independent palette of 8 colors out of 8192 colors and 8 transparent levels
- Up to 360x576 pixel of an overlay image rendered into 720x576 pixels
- Support H / V 2x scale mode
- Support blinking / timeout function

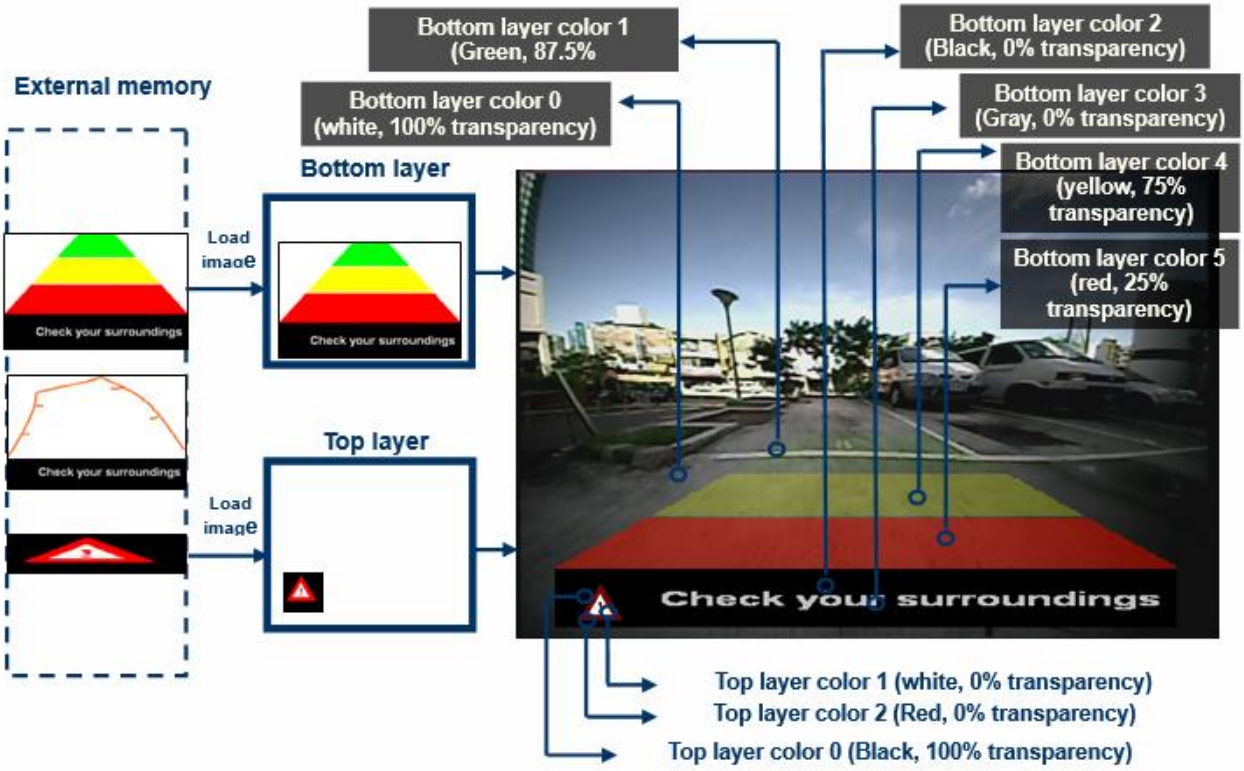


Figure 4.8: Overlay engine example (HM0435)

4.16. Digital window

Digital window adjusts the frame output to any size and location. The frame timing remains unchanged.

- Programming window size by specifying x **(horizontal)** and y **(vertical)** starting and ending position
  - X Start: **YUV_WINX_ST_HB[1:0], YUV_WINX_ST_LB[7:0]**
  - Y Start: **YUV_WINY_ST_HB[1:0], YUV_WINY_ST_LB[7:0]**
  - X End: **YUV_WINX_ED_HB[1:0], YUV_WINX_ED_LB[7:0]**
  - Y End: **YUV_WINY_ED_HB[1:0], YUV_WINY_ED_LB[7:0]**
- X Start / Y Start have to be an even number of pixels.
- The digital ISP has line buffers, so the register settings **(Y Start / Y End)** of digital output window has 4 lines delay with the actual physical position.

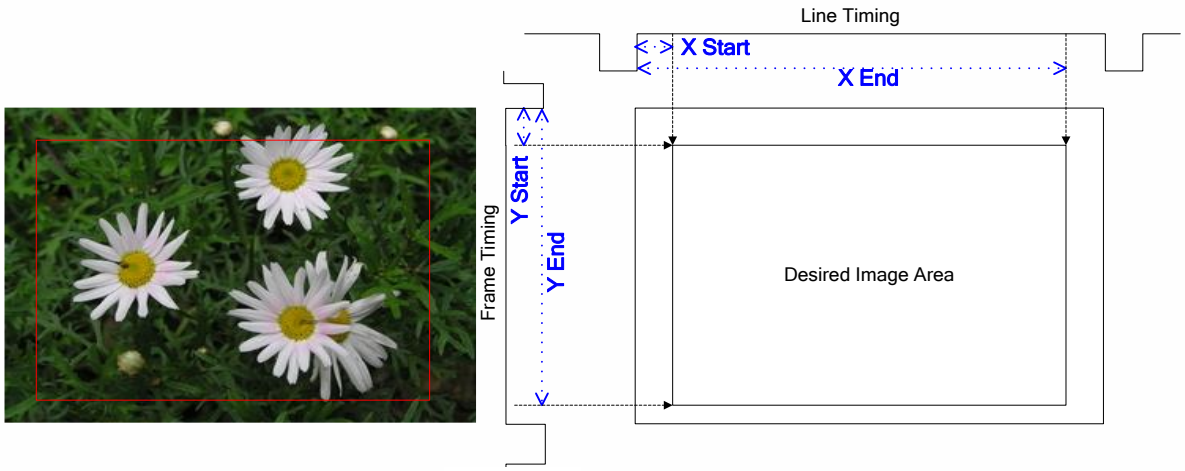


Figure 4.9: Windowing

4.17. Resolution and Scaling and Windowing

HM0435 supports NTSC0 / NTSC1 / NTSC2 / PAL0 / PAL1 readout mode via serial register programming.

HM0435 ISP need border pixels for calculation, and the register settings of digital window of different resolution are suggested to set as the following table that there are 4 border pixels of each side.

Resolution (Read out)	RDCFG 0x0006[3:2]	YUV / SCX 0x05E1 / 0x05E0	YUV / SCY 0x05E3 / 0x05E2	X-Start 0x05E5 / 0x05E4	X-End 0x05E7 / 0x05E6	Y-Start 0x05E9 / 0x05E8	Y-End 0x05EB / 0x05EA
NTSC0 (640x480)	01	0x7309	0x8000	0x0004	0x0283	0x0008	0x01E7
NTSC1 (714x536)	01	0x7EEE	0x8E66	0x0004	0x02CD	0x0008	0x021F
NTSC2 (720x536)	01	0x8000	0x8E66	0x0004	0x02D3	0x0008	0x021F
PAL0 (706x530)	01	0x7D82	0x75F7	0x0004	0x02C5	0x0008	0x0219
PAL1 (720x530)	01	0x8000	0x75F7	0x0004	0x02D3	0x0008	0x0219

Table 4.3: Digital window settings of different resolutions

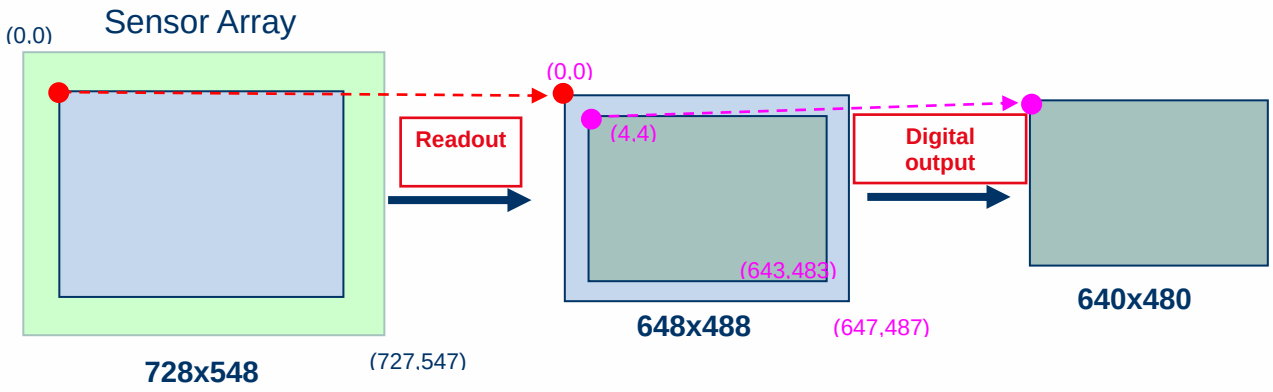


Figure 4.10: Depiction of NTSC0 digital window

4.18. Automatic Exposure (AE)

The Automatic Exposure analyzes the brightness statistics of the frame and adjusts the exposure and gain of the sensor to a programmed target value.

- AE statistic engine is comprised of 16 windows and the weighted average of all windows is calculated to compute the scene's brightness value. The starting location and the horizontal and vertical size of the window are programmable, and the weight of each window is individually programmable.
- Once the measured brightness is obtained, it is compared to the user programmable target brightness. The AE algorithm then computes the new exposure gain product value and determines the distribution of analog gain, digital gain and exposure.
- The AE can be bypassed through the serial register by setting register bit **AEWBCFG[0]** to 0.

4.19. Automatic White Balance (AWB)

Automatic White Balance **(AWB)** block adjusts the color gain of the sensor under different color temperatures based on the white pixel region of the scene based on color temperature estimation. The AWB can be bypassed through the serial register by setting register bit **AEWBCFG[1]** to 0. Each color gain can be manually programmed.

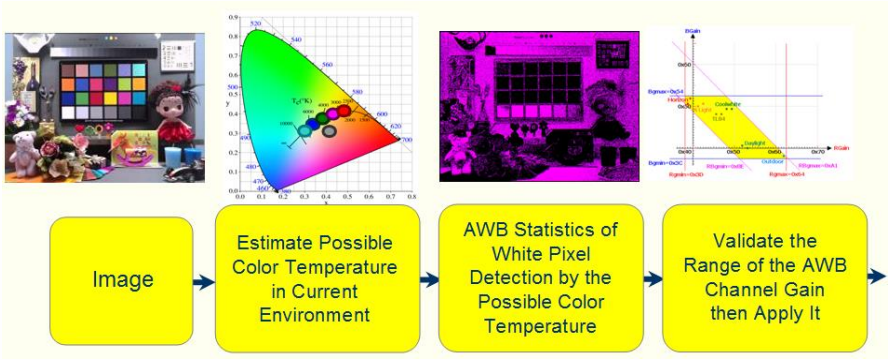


Figure 4.11: AWB algorithm flow diagram

4.20. ClearView™ Optical Restoration Engine (ORE)

An Optical Restoration Engine **(ORE)** with ClearView™ technology provides lens-based compensation to deal with the inevitable loss of sharpness and details induced by camera optics. ClearView™ calibration quickly adapts the Optical Restoration Engine to the properties of the lens.

4.21. Auto-flicker detection

On-chip auto-flicker detection automatically detects the frequency of fluorescent light source **(50Hz/60Hz)** and selects the appropriate integration time interval of the Automatic Exposure.

4.22. Special effects

HM0435 features several pre-defined modes for fast access of the special effects: sketch, emboss, solarization, negative, monochrome and fixed Y with U and V staying adjustable.

4.23. Auto-boot function

HM0435 supports Auto-boot function. After power is supplied, the HM0435 will enter a boot sequence to configure its operating mode. The detailed flow chart is depicted in the following figure. After power is supplied or reset, HM0435 will sample bootstrap pins and try to read HII multi-byte tags form SPI devices. Then it will configure itself by bootstrap pin values and data in SPI memory or/and OTP.

Chip functions are automatically selected according to bootstrap pins with pull-up or pull-down. The detailed function options by bootstrap pins are listed in following table. The default selections are indicated by bold font.

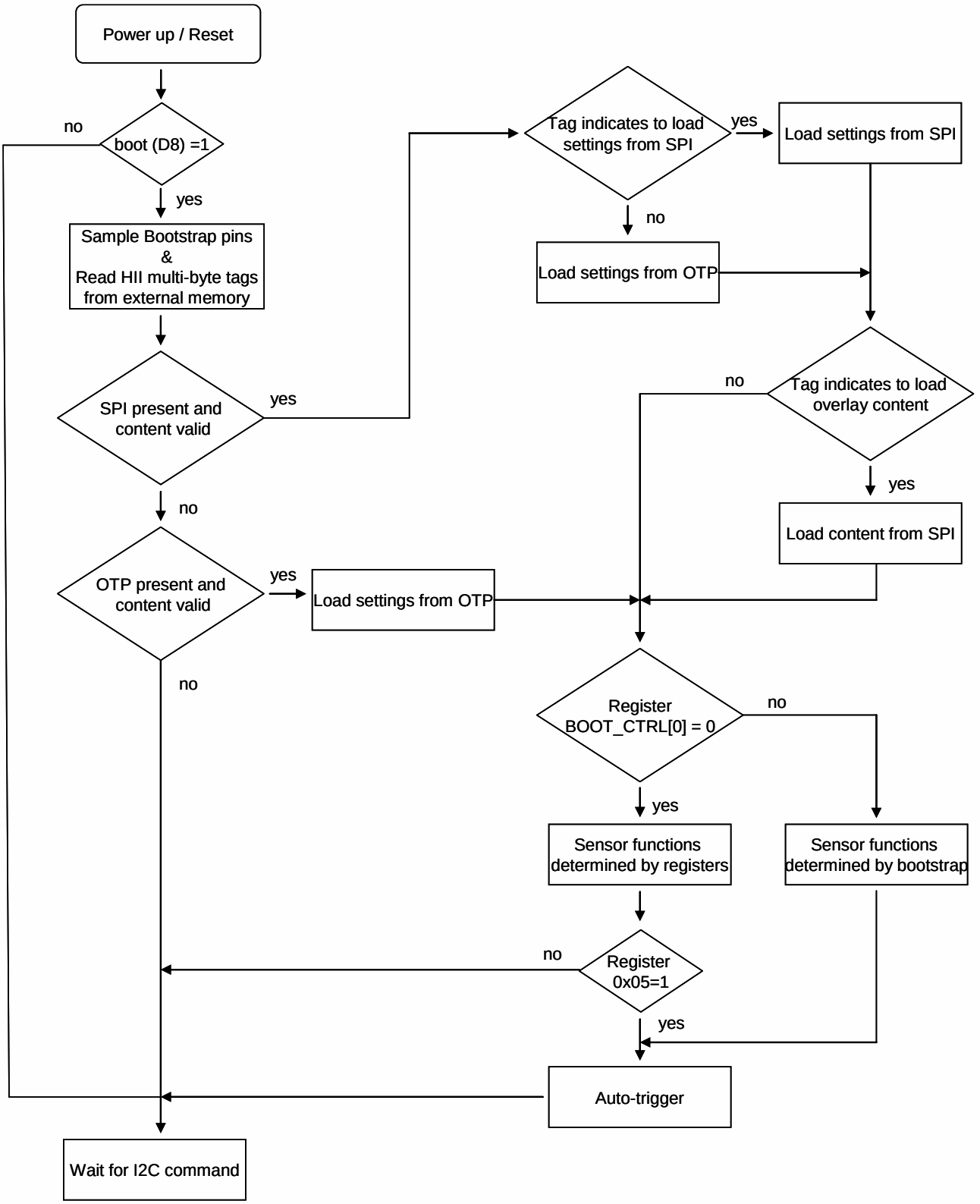


Figure 4.12: Auto-boot flow chart

		OVEN	VSYNC	HSYNC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
Overlay	Disable	L	-	-	-	-	-	-	-	-	-	-	-	-
	Enable	H	-	-	-	-	-	-	-	-	-	-	-	-
Flicker	60Hz mode	-	L	L	-	-	-	-	-	-	-	-	-	-
	50Hz mode	-	L	H	-	-	-	-	-	-	-	-	-	-
	Auto mode	-	H	-	-	-	-	-	-	-	-	-	-	-
SPI Memory	Flash	-	-	-	L	-	-	-	-	-	-	-	-	-
	EEPROM	-	-	-	H	-	-	-	-	-	-	-	-	-
TV System	NTSC	-	-	-	-	L	L	L	L	-	-	-	-	-
	PAL	-	-	-	-	H	L	L	L	-	-	-	-	-
I2C Bus Address	0x24 (7-bit)	-	-	-	-	-	-	-	-	L	-	-	-	-
	0x34 (7-bit)	-	-	-	-	-	-	-	-	H	-	-	-	-
Horizontal Mirror	Disable	-	-	-	-	-	-	-	-	-	L	-	-	-
	Enable	-	-	-	-	-	-	-	-	-	H	-	-	-
Vertical Flip	Disable	-	-	-	-	-	-	-	-	-	-	L	-	-
	Enable	-	-	-	-	-	-	-	-	-	-	H	-	-
Boot Mode	Manual mode	-	-	-	-	-	-	-	-	-	-	-	L	-
	Auto mode	-	-	-	-	-	-	-	-	-	-	-	H	-
Black/White mode	Disable	-	-	-	-	-	-	-	-	-	-	-	-	L
	Enable	-	-	-	-	-	-	-	-	-	-	-	-	H

Table 4.4: Chip function selection by bootstrap pins

4.24. Controllable black-white output function

HM0435 supports working with ICR. When the external controller enables IR-LED and switches IR-cut, the external controller can output control signal **(GPIO)** to control HM0435 output black and white signal.

5. Typical Application Circuit

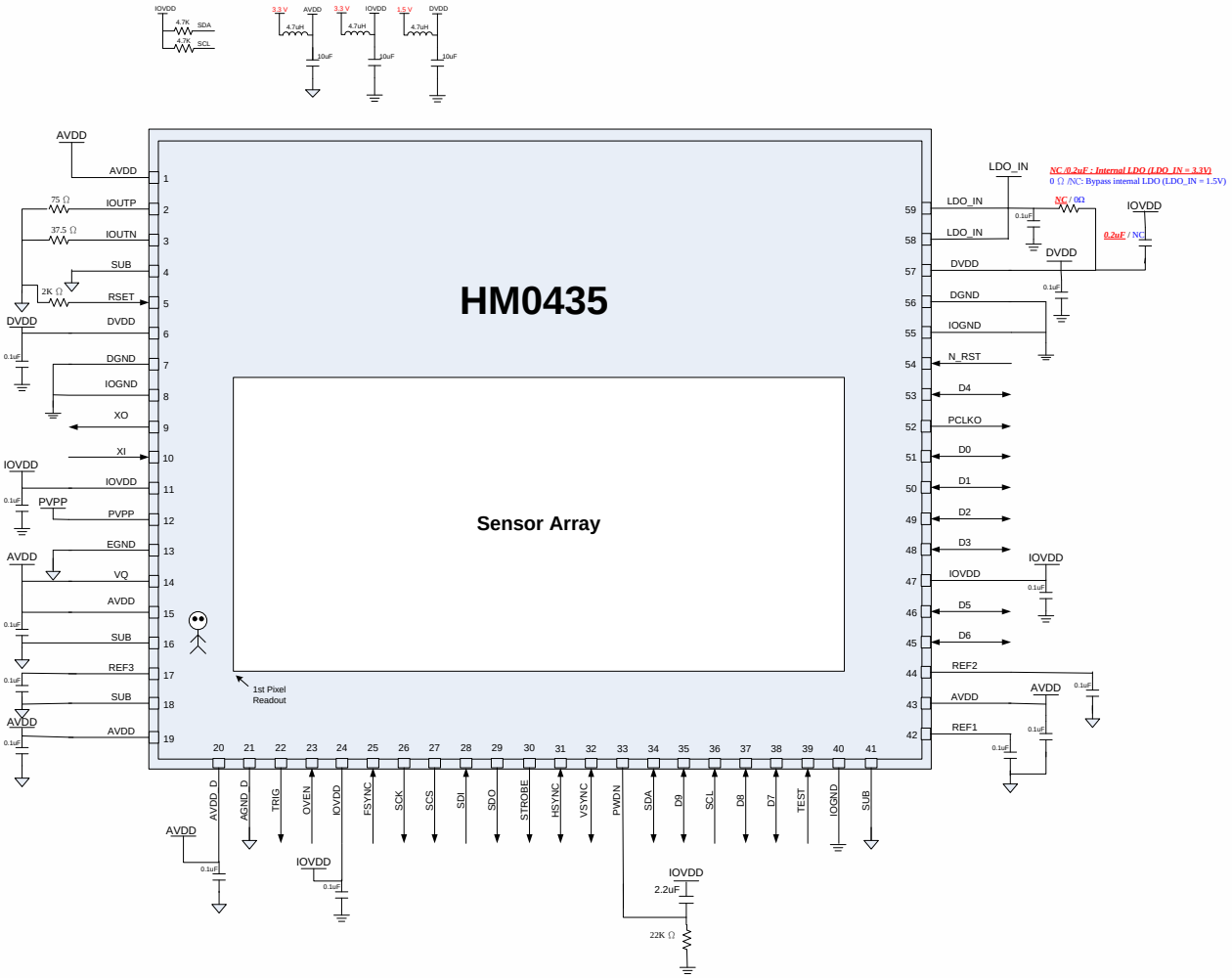


Figure 5.1: Application circuit for Bare Die

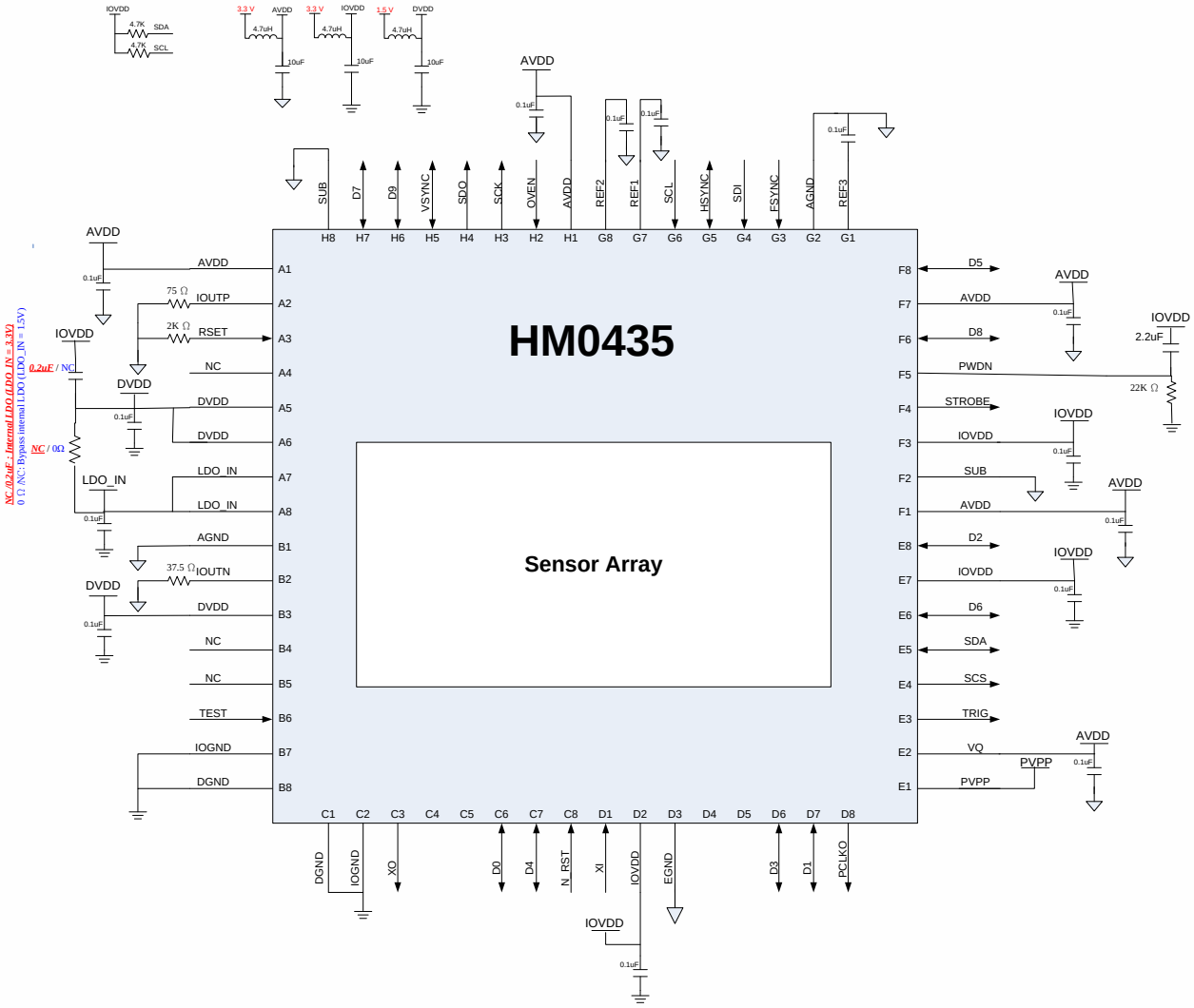


Figure 5.2: Application circuit for CSP

6. System Level Description

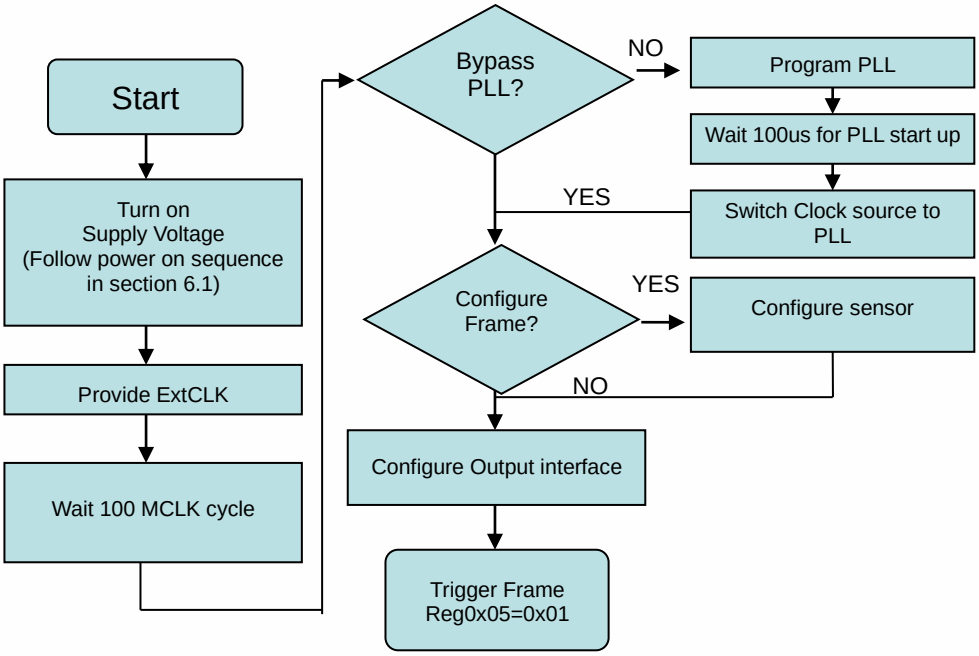


Figure 6.1: Sensor Power up sequence

6.1. Supply voltage sequence

As a general guideline, the IOVDD supply should be powered up first or at the same time with respect to AVDD and DVDD. An on-chip power-on reset pulse is applied to the digital core and ensures that internal register values are initialized correctly to the default values.

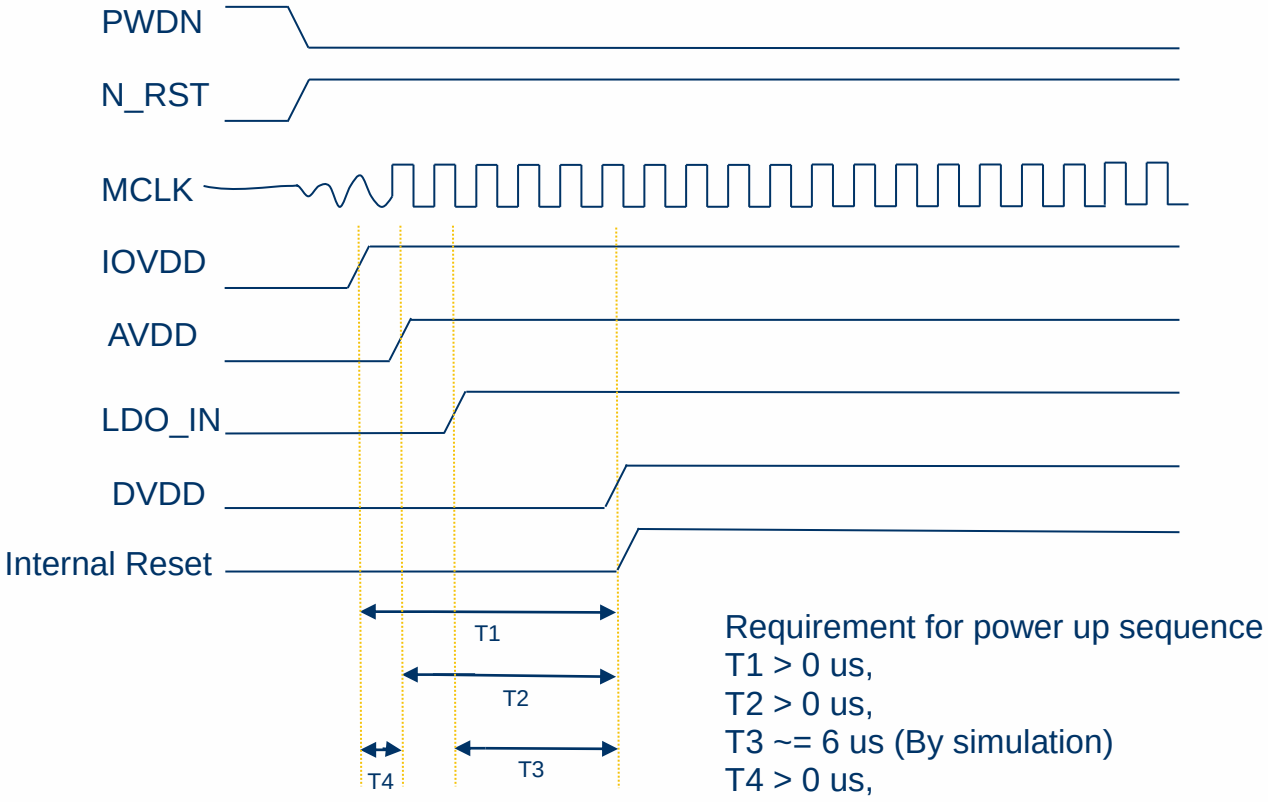


Figure 6.2: Power up sequence using POR

The suggested method is to delay and release PWDN signal when all power supplies have settled to the recommended operating voltage.

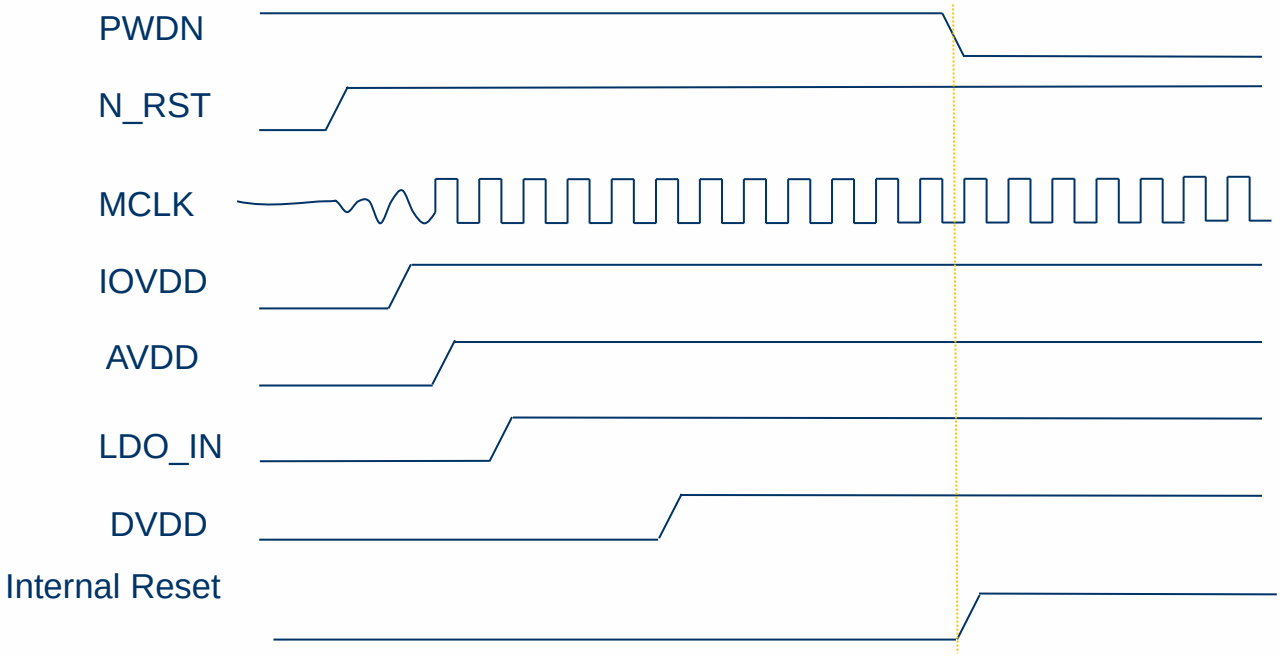


Figure 6.3: Power up sequence using external control

6.2. Clock generation

The sensor system clock can be set by the on-chip Phase Lock Loop or direct from the external clock source.

- A frequency divider is programmed based on the input clock; the input of the PLL can be 3MHz, 6MHz, 9MHz, 12MHz, … 48MHz.
- The PLL output frequency is set by the programmable frequency multiplier.
- PLL can be bypassed by setting **CKCFG[7]** to 1. By default, PLL is powered down after power up. PLL must be enabled by **PLLCFG[5]** and clock source can be switched to PLL by first programming the PLL frequency selection registers **CKCFG**, **PLLCFG**, **PLL1CFG**, **PLL2CFG** and then writing **CKCFG[7]** to 0.

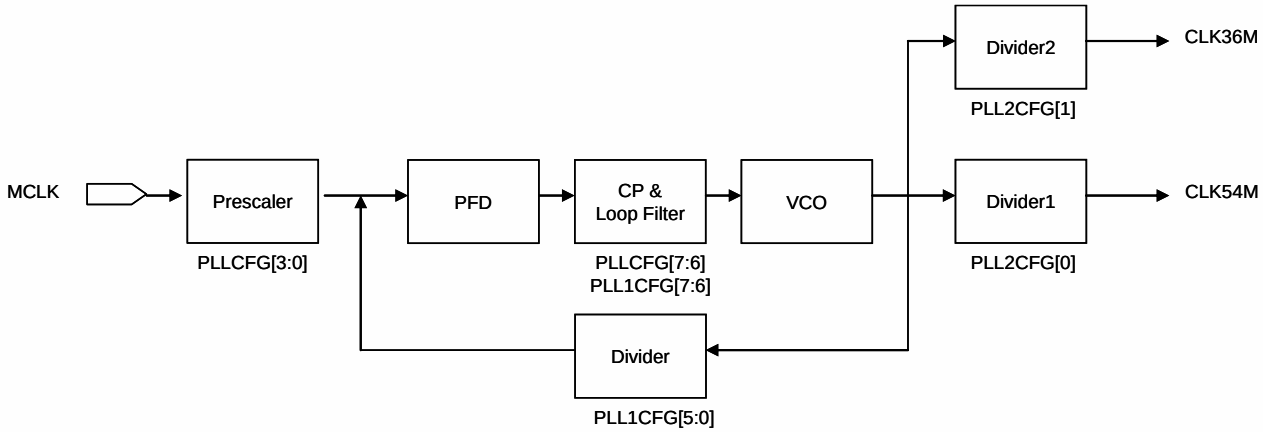


Figure 6.4: Clock generator

6.3. Power down

Two Power down modes are available in the sensor:

- Hardware Power down
  - Initiated by setting PWDN pin high.
  - Suspend circuits and stops internal system clock. All internal registers are reset.
- Soft Power down
  - Initiated by following sequence
    - First, set register **TGRDCFG[0]** = 0 to turn off rolling shutter.
    - Second, set register **PWDCTRL[7:0]** = 0x15h.
  - Following the sequence, the circuits are suspended at the end of the frame, and all internal register values are maintained.

6.4. Reset

Software reset and hardware reset options are available in the sensor.

- Software reset is set by programming 0x00h to **SFTRST[7:0]**
- Hardware reset is set by setting N_RST pin low.

7. Serial Interface Description

7.1. I2C bus

The 2-Wire serial interface provides read/write access to the sensor registers

- 2-Wire serial interface consists of SDA **(bidirectional serial data)** and SCL **(serial clock)** pins.
- If D5 pin is pulled down, the slave device ID is 8-bit 0x48h **(Write ID)** and 0x49h **(Read ID)**.
- If D5 pin is pulled up, the slave device ID is 8-bit 0x68h **(Write ID)** and 0x69h **(Read ID)**.
- HM0435 uses 16-bit register address and 8-bit register data.
- The sensor uses double-buffered registers to ensure that register changes that affect sensor operation takes place at the beginning of the next valid video frame.
- The host generates SCL clock signal to the sensor and uses the signal to synchronize all data transfer.

7.1.1. Start / Stop conditions

The Start and Stop conditions on the serial bus is issued by the Host.

SDA Transition	SCL	Condition
High to Low	High	Start
Low to High	High	Stop

Table 7.1: 2-Wire serial interface Start / Stop transition

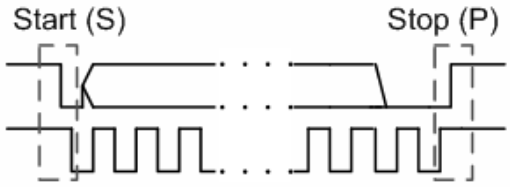


Figure 7.1: 2-Wire serial interface Start / Stop condition

7.1.2. Data valid

One SCL pulse is generated for each data bit transferred. The host should ensure that the SDA signal must be stable when SCL in High. The SDA signal can transition when SCL is Low.

7.1.3. Data format

Data is transferred one byte at a time. The most significant bit should always be transferred first. Each byte is followed by an acknowledgement **(ACK)** or a no-acknowledgement bit **(No ACK)**.

7.1.4. Acknowledge / No-Acknowledgement

Each 8-bit is followed by an Acknowledge **(ACK)** or No-Acknowledge **(No ACK)** bit.

- Acknowledge: The Host will release the SDA line. The sensor will drive the SDA line low.
- No-Acknowledge: The Host will release the SDA line. The sensor will not drive the SDA pin **(Pulled high)**. The No-Ack bit is used to terminate a read sequence.

7.1.5. Write sequence

- Initiated by Host with Start **(S)** condition, followed by 8-bit device slave ID **(Write ID)**
- If the slave ID is recognized by the sensor, the ACK bit will be sent to the Host.
- Once the Host receives an ACK from the sensor, it can begin to transmit the register address **(High byte first, then low byte)**, then the register data. After each byte, the sensor will issue an ACK or No ACK signal.
- The write operation is completed when the Host asserts a stop condition

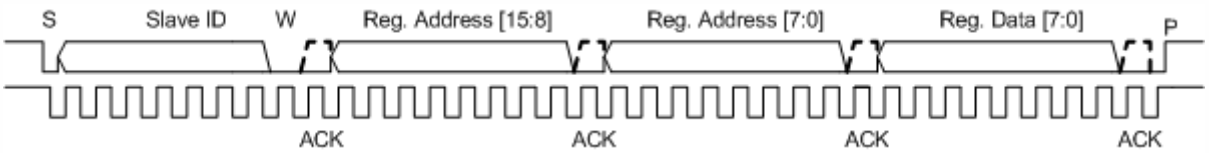


Figure 7.2: 2-Wire serial interface 16-bit address write

7.1.6. Read sequence

- Initiated by Host with Start **(S)** condition, followed by the 8-bit device slave ID **(Write ID)**.
- If the slave ID is recognized by the sensor, the ACK bit will be sent to the Host.
- Once the Host receives an ACK from the sensor, it can begin to transmit the register address **(High byte first, then low byte)**, then the register data. After each byte, the sensor will issue an ACK or No ACK bit.
- The write operation is completed when the Host asserts a Stop condition.
- The Host must issue another Start condition, followed by the 8-bit device slave ID **(Read ID)**.
- If the register ID is recognized by the sensor, the ACK bit will be sent to the Host.
- The sensor will respond with the Register Data Out.
- The Host will issue an ACK, and then asserts the Stop condition.

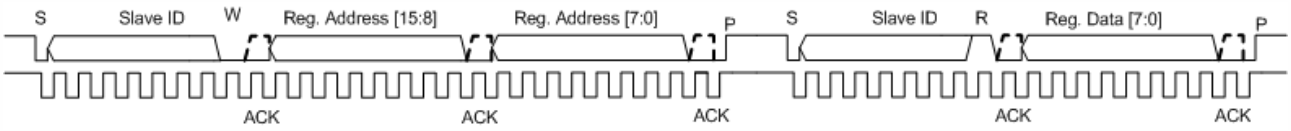


Figure 7.3: 2-Wire serial interface 16-bit address read

7.2. Serial Peripheral Interface (SPI)

HM0435 is embedded with a simply standard SPI Master which only supports read command. It is used to interface external memory to load overlay content and register settings. HM0435 supports in-system programming of SPI Flash/EEPROM. Pull down OVEN (**The SPI memory has code that set BOOT_CTRL[0]=1)** as depicted in following figure or set register **IOCNTR3[4:3]**=0 through I2C interface , then all four pins of SPI will be tri-stated, thus enabling external SPI Programmer to program the Flash /EEPROM.

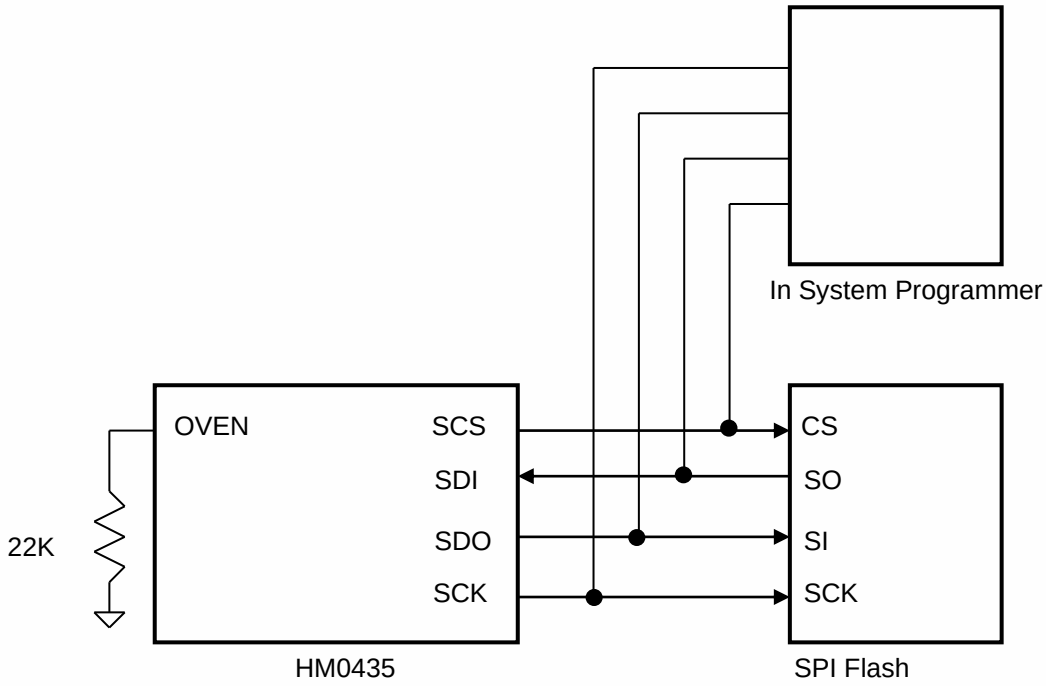


Figure 7.4: SPI bus with in system programmer

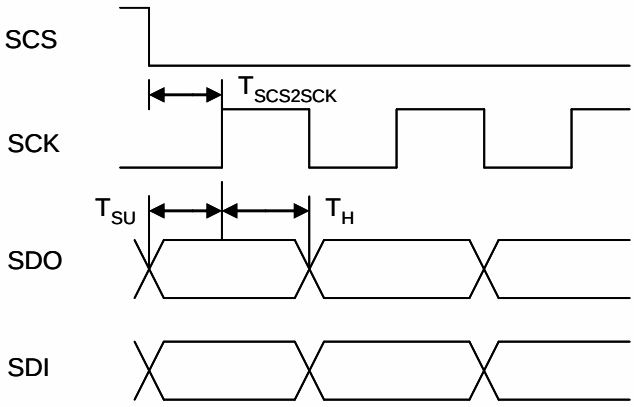


Figure 7.5: SPI timing diagram

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
SPI SCK frequency	f_{SPI_CLOCK}	-	3.375	-	MHz
SCS setup time	$T_{SCS2SCK}$	-	148	-	ns
Setup time	T_{SU}	-	-	148	ns
Hold time	T_H	-	-	148	ns

Table 7.2: SPI output timing

8. Digital Output Format and IO Control

8.1. Output format

The HM0435 supports RAW10, YCbCr, RGB 565/555/444 and ITU BT.656. The data format is select through **OUTPORTCONTROL[7:0]** register.

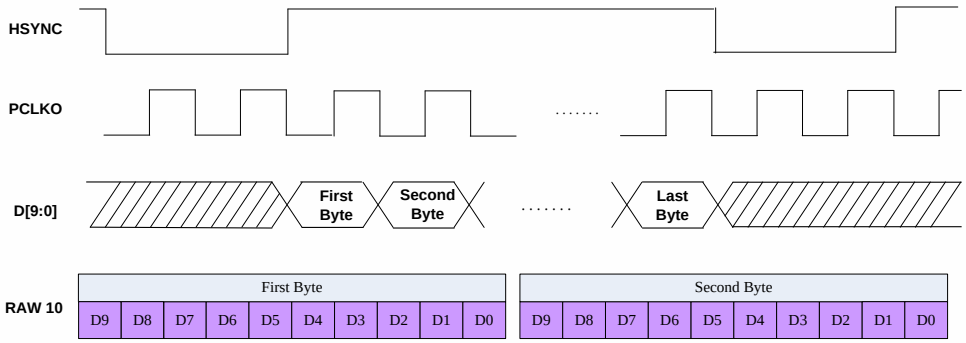


Figure 8.1: RAW output format

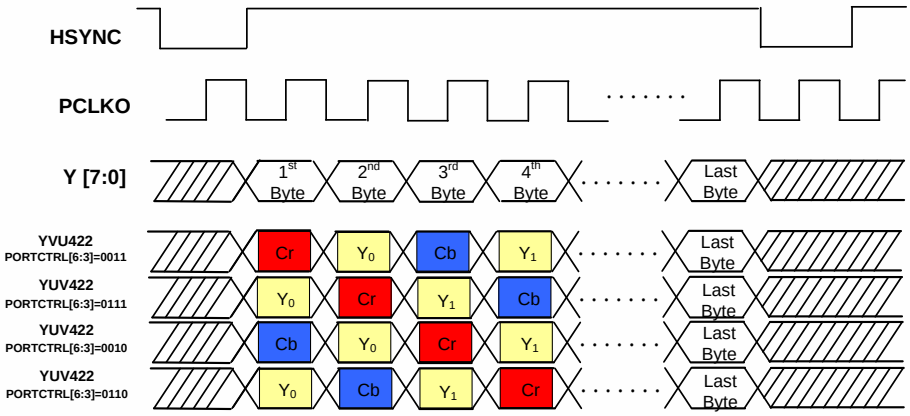


Figure 8.2: YCbCr output format

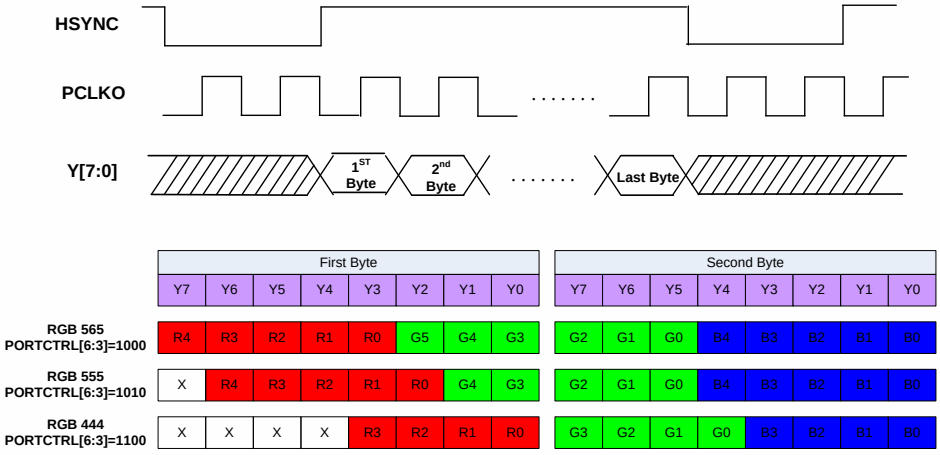


Figure 8.3: RGB 565 / 555 /444 output format

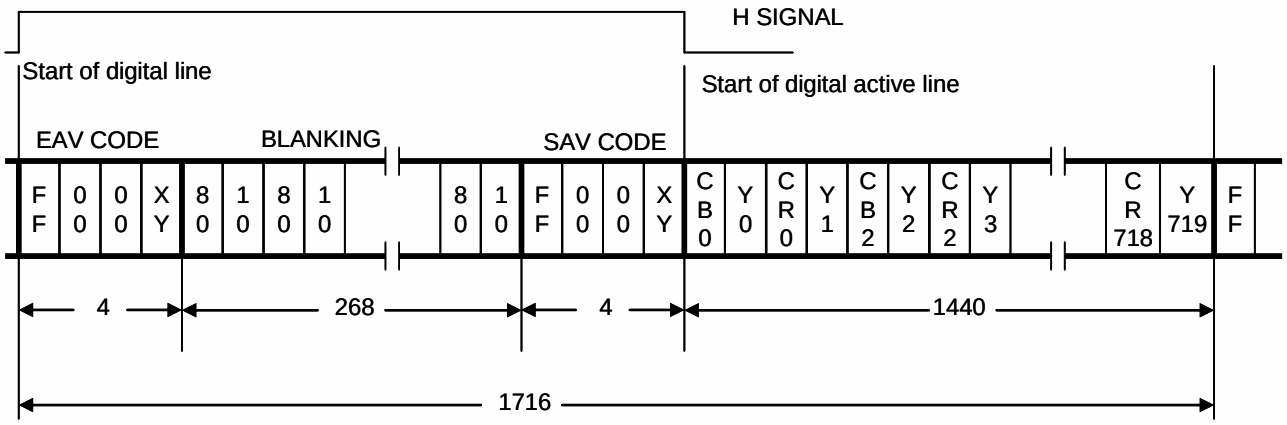
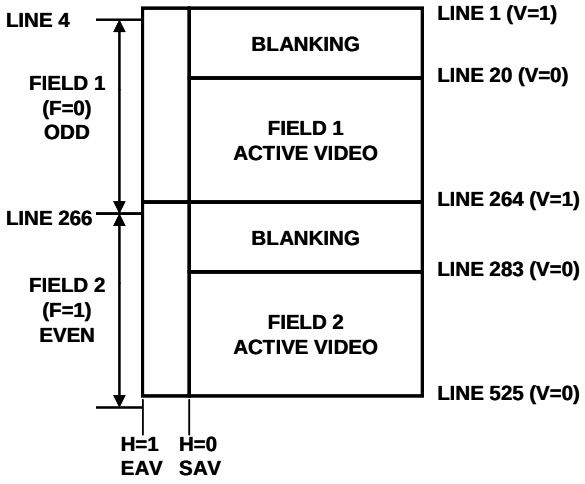


Figure 8.4: BT.656 8-bit parallel interface data format for 525/60 video system



LINE NUMBER	F	V	H (SAV)	H (EAV)
1-3	1	1	1	0
4-19	0	1	1	0
20-263	0	0	1	0
264-265	0	1	1	0
266-282	1	1	1	0
283-525	1	0	1	0

Figure 8.5: BT.656 vertical blanking intervals for 525/60 video system

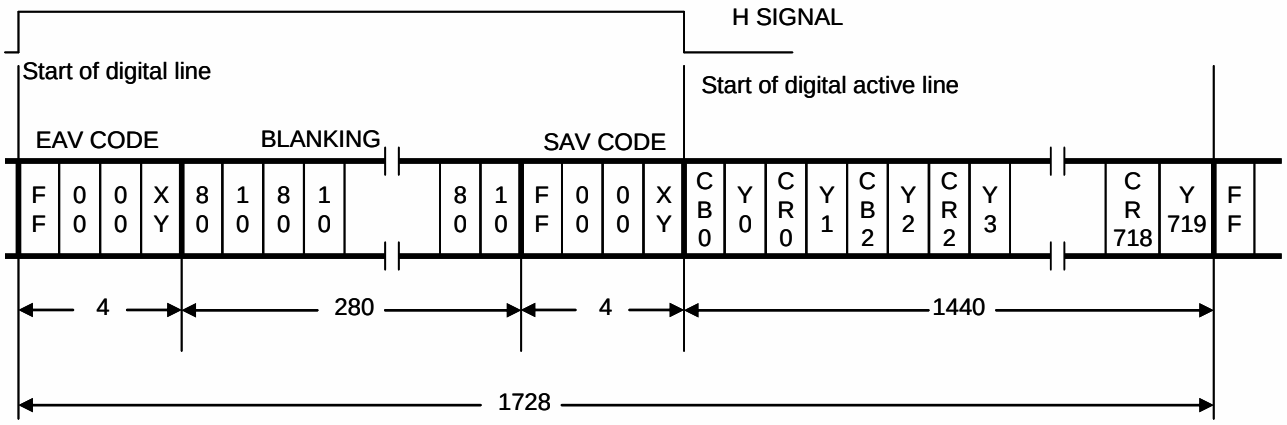
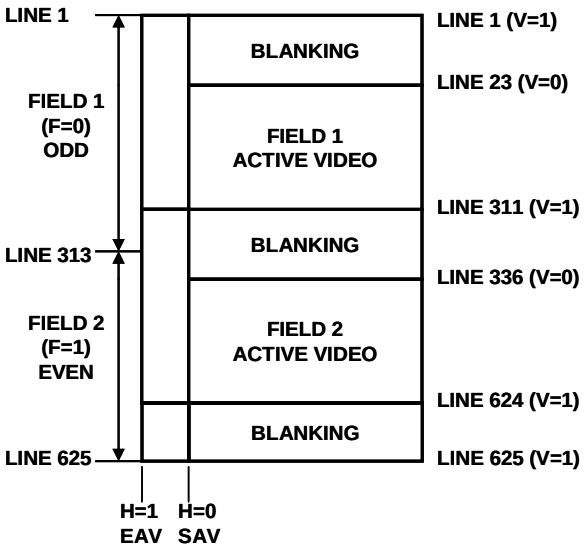


Figure 8.6: BT.656 8-bit parallel interface data format for 625/50 video system



LINE NUMBER	F	V	H (SAV)	H (EAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

Figure 8.7: BT.656 vertical blanking intervals for 625/50 video system

8.2. I/O control

8.2.1. Output enable

When not in use, the I/O pins **(Video synchronization, data bus)** can be tri-stated allowing multiple devices to share the same bus.

IOCNTR[3][7]	Output State
0 **(Default)**	**Tri-state enable**
1	**Output enable**

Table 8.1: Output enable control truth table

8.2.2. IO control

The IO drive current and polarity can be configured to meet a wide array of system requirements. The IO signals are synchronized to the PCLKO output. By default, the data signal transitions on the falling edge of PCLKO. This allows the user to latch data on the subsequent rising edge of PCLKO.

IO Pad	Drive	Polarity Control	Default Polarity [OPRTCFG bit value]
PCLK	IOCNTRH[6:4]	OPRTCFG[5]	Data transition on falling edge [0]
D0-D4	-	-	-
D5-D9	IOCNTRH[2:0]	-	-
VSYNC	-	OPRTCFG[6]	Active High [0]
HSYNC	-	OPRTCFG[7]	Active High [0]
PCLK	IOCNTRH[6:4]	OPRTCFG[5]	Data transition on falling edge [0]
D0-D4		-	-
D5-D9	IOCNTRH[2:0]	-	-
VSYNC		OPRTCFG[6]	Active High [0]
HSYNC		OPRTCFG[7]	Active High [0]

Table 8.2: IO control

8.2.3. Gated Pixel Clock

The pixel clock **(PCLKO)** can be gated by HSYNC signal by setting register bit **CKGATECTRL[2]** to 1 and can be gated by VSYNC by setting register bit **CKGATECTRL[3]** to 1.

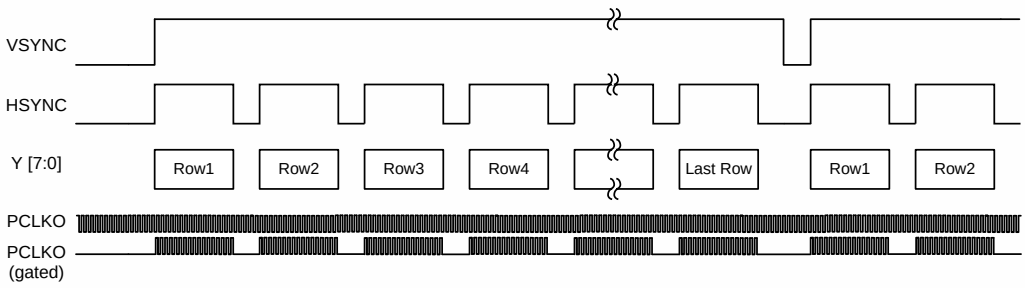


Figure 8.8: Gated pixel clock

9. Composite Video Output Mode

9.1. NTSC

The NTSC format is supported with 480 active image rows. The HM0435 support both differential and single-ended configuration of the NTSC format. The differential configuration provides better noise performance suitable for long distance application. The single-ended configuration is well-suited in system design with high noise immunity.

9.2. PAL

The PAL format is supported with 576 active image rows. The HM0435 support both differential and single-ended configuration of the PAL format. The differential configuration provides better noise performance suitable for long distance application. The single-ended configuration is well-suited in system design with high noise immunity.

10. Frame Timing and Control

10.1. Command update

Serial registers that are synchronized to sensor timing utilize double-buffer register to ensure that changes take effect at the start of a subsequent frame. In the **Register table** section of this document, the registers that require Command Update, such as integration and gain, are indicated by the type designator **CMU_RW**.

The sequence is as follows:

- User writes to the target serial register**(s)** where the value will be stored in the first buffer.
- User issues Command Update **(CMU)** by writing any non-zero value to CMU[7:0] register. The register values will be moved to the second register buffer
- If the double-buffer registers and CMU are issued before frame trigger, the first frame **(Frame n)** will apply the new values.
- If the CMU is issued after the frame trigger, the first frame using the new settings will be Frame n+2. The settings for Frame n+1 may use the current settings or new settings depending on the CMU relative to the internal start of the next frame.
- Note there are no bad frames such that two settings may be applied to a single frame. Should the new setting be applied to Frame n + 2, then Frame n+1 would simply use the previous settings.

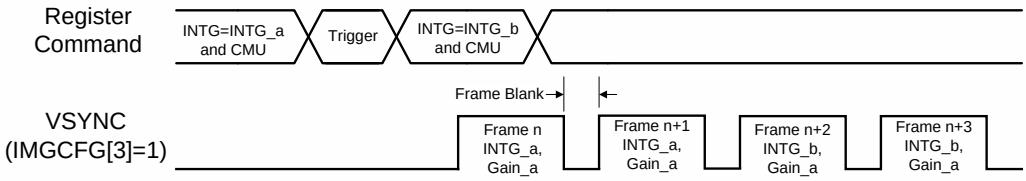


Figure 10.1: Command Update (CMU) of integration time and gain value change

10.2. Frame rate control

The frame rate is the frequency which sensors produces consecutive images and can be accurately measured using the VSYNC signal. The HM0435 supports both Fixed Frame Rate and Variable Frame Rate mode.

- Fixed Frame Rate mode
  - Fixed Frame Rate mode is selected by setting register bit **IMGCFG[3]** = 1.
  - In Fixed Frame Rate mode, the VSYNC period is always fixed.
    - Maximum lines of integration = Frame Height
    - ***Note that the sensor will only apply the maximum lines of integration for any programmed value greater than the maximum lines of integration.***
  - The frame rate can be calculated by ***Frame rate = 1 / (t_{LINE} × Frame Height)*** Where
    - t_{LINE} = (**TOTALROW_H[7:0]**×2^8 + **TOTALROW_L[7:0]**)/2 × t_{pixel}
    - t_{pixel} = 2 × t_{PCLKO} for YUV and t_{pixel} = t_{PCLKO} for raw data
    - Frame Height = 28 + Active Rows + ROW BLANK (**BLNKR_H[7:0]** × 2^8 + **BLNKR_L[7:0]**)

- Variable Frame Rate mode
  - Variable Frame Rate mode is selected by setting **IMGCFG[3]** = 0 **(Default)**
  - The VSYNC period is fixed except for one frame when a new applied integration value is greater than previous integration value.
  - Maximum lines of integration is 65535
  - The frame rate can be calculated by ***Frame rate = 1 / (t_{LINE} × Frame Height)*** Where
    - t_{LINE} = (**TOTALROW_H[7:0]**×2^8 + **TOTALROW_L[7:0]**)/2 ×t_{pixel}
    - t_{pixel} = 2 × t_{PCLKO} for YUV and t_{pixel} = t_{PCLKO} for raw data
    - Frame Height (Integration Time <= (28 + Active Rows + ROW BLANK-2)) = 28 + Active Rows + ROW BLANK (**BLNKR_H[7:0]** × 2^8 + **BLNKR_L[7:0]**)
    - Frame Height (Integration Time > (28 + Active Rows + ROW BLANK-2)) = Lines of Integration ((**INTGH[7:0]** × 2^8 + **INTGL[7:0]**)) + 4

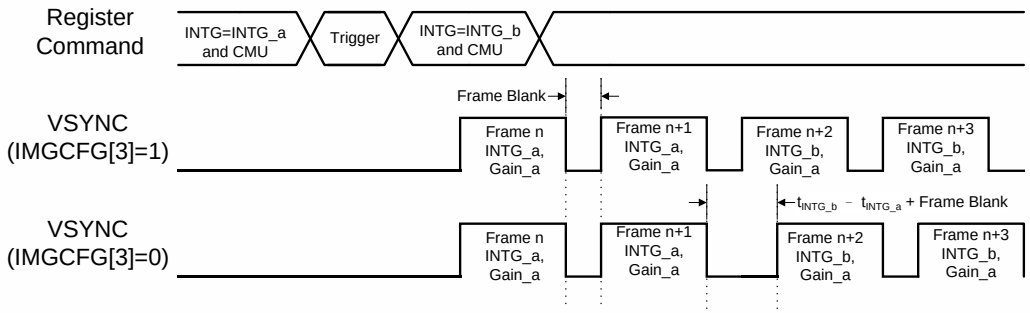


Figure 10.2: Fixed and Variable frame rate mode

10.3. Exposure control

In rolling shutter operation, the sensor resets each row of pixel sequentially starting from the first row. After reset, each row of pixels begins to integrate light, and at the end of the integration time **(Also known as exposure time)**, the row is read out sequentially at the same rate as the reset process.

The total integration time can be calculated by the following equation:

Total Integration Time = INTG × t_{LINE}

Where:

- INTG = (**INTGH [7:0]** × 2^8 + **INTGL [7:0])**
- t_{LINE} = (**TOTALROW_H[7:0]**×2^8 + **TOTALROW_L[7:0]**)/2 ×t_{pixel}
- t_{pixel} = 2 × t_{PCLKO} for YUV and t_{pixel} = t_{PCLKO} for raw data

10.4. Flicker step

The sensor should be programmed to use exposure intervals of 1/100 second for 50Hz flicker frequency and 1/120 second for 60Hz flicker frequency. The exposure intervals are used to avoid banding in fluorescent light condition.

As discussed in the previous Integration Time **(Exposure)** Control section, the integration time can be calculated by the following equation:

Total Integration Time = INTG × t_{LINE}

- INTG **(60Hz Flicker Step)** = (1/120) / t_{LINE}
- INTG **(50Hz Flicker Step)** = (1/100) / t_{LINE}

10.5. Analog gain control

The HM0435 provides global analog gain based on the following equation:

Analog gain = 2^**AGAIN[2:0]**

10.6. Digital gain control

The HM0435 provides global digital gain based on the following equation:

Digital gain = **DGAIN[7:0]** / 64

10.7. Trigger control

Frame can be triggered for either multiple frames or single snapshot by setting the trigger register **TGRDCFG[0]** = 1.

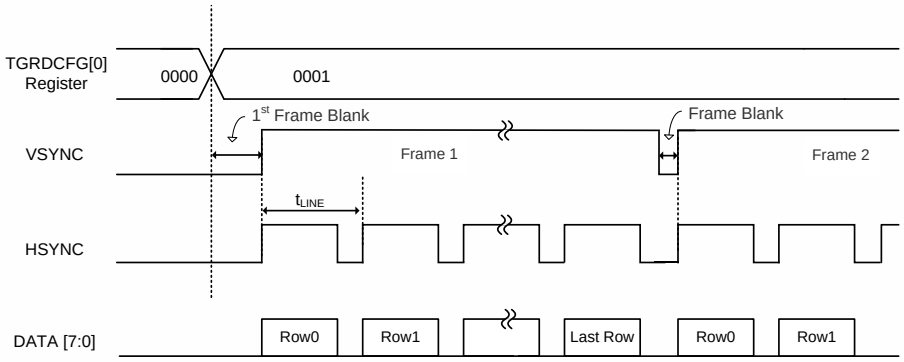


Figure 10.3: Rolling shutter / Continuous frame

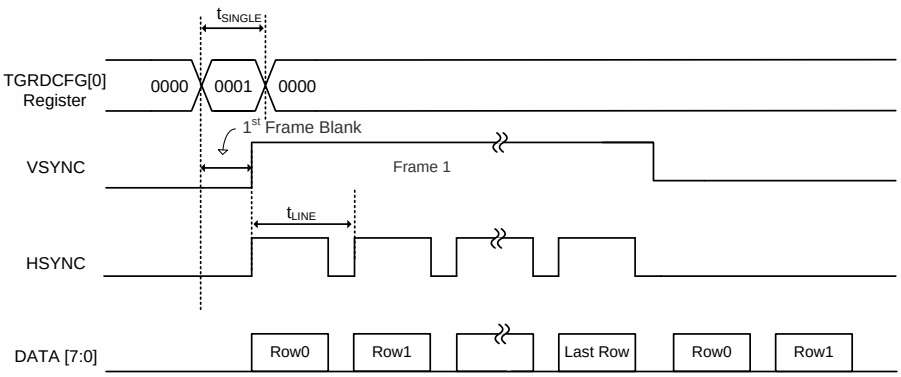


Figure 10.4: Rolling shutter / Single frame

11. Register Table

- There are 3 types of registers, Read-Write **(RW)**, Read-Only **(RO)** and Write-Only **(WO)** registers.
- Registers that require Command Update are indicated by **CMU_RW.**
- Writing to reserved and unlisted registers will cause undefined sensor behavior.
- All default settings are indicated in bold.

11.1. Chip ID / Power down control registers [0x0000 – 0x000F]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0000	[7:0]	CMU	WO	Command Update	NA
0x0001	[7:0]	CHPIDH	RO	Chip ID High Byte	0x04
0x0002	[7:0]	CHPIDL	RO	Chip ID Low Byte	0x45
0x0003	[7:0]	CHPVID	RO	Chip Version ID	-
0x0004	[7:5] [4:0]	PWDCTRL	RW	Power Down Control [7:5]: NA [4]: I2C power down mode 0: Disable 1: Enable [3]: NA [2]: Digital power down **(Software power down)** 0: Normal 1: Power down [1]: Analog power down 0: Normal 1: Power down [0]: LDO power down 0: Normal 1: Power down	0x10
0x0005	[7:0]	TGRDCFG	RW	Trigger Configuration and Imager Readout Configuration [7:1]: Reserved. Must set to 0 [0]: Trigger configuration mode 0: No video 1: Rolling shutter, video mode	0x00
0x0006	[7:0]	RDCFG	CMU_RW	Imager Readout Configuration [7:4]: NA [3:2]: Fixed window enable 00: Full frame 01: arbitrary window readout Others: NA **(Cannot be used)** [1]: Horizontal mirror enable 0: Normal forward 1: Mirror **(Reverse h-readout)** [0]: Vertical mirror enable 0: Normal forward 1: Flip **(Reverse v-readout)**	0x04
0x000B	[7:0]	RESERVED	RW	Reserved	0x00
0x000C	[1:0]	RESERVED	RW	Reserved	0x00
0x000D	[7:0]	VREAD	CMU_RW	Imager Vertical Reading Out Mode [7:1]: NA [0]: Vertical sub-sampling mode	0x00
0x000E	[7:0]	HREAD	CMU_RW	Imager Horizontal Reading Out Mode [7:1]: NA [0]: Horizontal sub-sampling mode	0x00
0x000F	[7:0]	IMGCFG	CMU_RW	Imager Output Configuration [7:6]: NA [5]: Reserved [4]: Fixed row length 0: High speed readout 1: Fixed row length [3]: Fixed frame rate enable **(When select NTSC or PAL will force it to fix frame rate)** 0: non fixed frame rate mode 1: Fixed frame rate [2]: synchronize updating AWB and updating AE [1]: OUTFRAMEDELAY **(0x77)** enable [0]: Unused	0x18

11.2. Image operation registers [0x0010 – 0x001D]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0010	[7:0]	BLNKR_H	CMU_RW	Blanking Row MSB [7:0]: LSB = 1 row	0x00
0x0011	[7:0]	BLNKR_L	CMU_RW	Blanking Row LSB [7:0]: minimum is 2 rows	0x09
0x0012	[7:0]	RESERVED	-	Reserved	0x09
0x0013	[7:0]	RESERVED	-	Reserved	0x01
0x0014	[7:0]	RESERVED	-	Reserved	0x01
0x0015	[7:0]	INTGH	CMU_RW	[7:0]: Image Integration Time Setting MSB	0x01
0x0016	[7:0]	INTGL	CMU_RW	[7:0]: Image Integration Time Setting LSB	0x08
0x0017	[7:0]	RESERVED	-	Reserved	0x00
0x0018	[3:0]	AGAIN	CMU_RW	Analog Coarse Global Gain Gain=2^AGAIN[2:0] [3]: NA [2:0]: AGAIN 000: 1x 001: 2x 010: 4x 011: 8x 100: 16x	0x00
0x001D	[7:0]	DGAIN	CMU_RW	[7:0]: AE Digital Global Gain; Format 2.6 Gain=DGAIN[7:0]/64	0x40

11.3. Global control registers [0x0020 – 0x002F]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0020	[7:0]	OPRTCFG	RW	Output Polarity Configuration [7]: Hsync Display 0: Active-high 1: Active-low [6]: Vsync Display 0: Active-high 1: Active-low [5]: PCLK Display 0: Transition on falling edge 1: Transition on rising edge [4]: Unused [3]: AE frame rate control 0: Normal AE control 1: Frame rate AE control [2]: Reserved [1]: Reserved [0]: Reserved	0x00
0x0022	[7:0]	SFTRST	WO	Software Reset	0x00
0x0023	[7:0]	IOCNTRH	RW	IOs Control Configuration; high byte [7]: Output tri-state disable **(VSYNC, HSYNC, D9~D5)** 0: Tri-state 1: Non tri-state [6:4]: Clock pad drive strength [3]: Output tri-state disable **(D4~D0)** 0: Tri-state 1: Non tri-state [2:0]: Data pad drive strength	0x43
0x0024	[7:0]	CKGATECTRL	RW	[7]: Reserved [6]: NA [5] PCLK_Raw neg. edge [4]: NA [3]: PCLK Display Gated by Vsync 0: Not gated 1: Gated by Vsync [2]: PCLK Display Gated by Hsync 0: Not gated 1: Gated by Hsync [1:0]: Reserved	0x00
0x0025	[7:0]	CKCFG	RW	[7]: digital clock source selection 0: PLL 1: System clock [6:0]: divider for digital clock PCLK = clock selected by R_CKCFG [7] / (R_CKCFG[6:0] + 1)	0x80

Address	Byte	Register name	Type	Description	Default (Hex)
0x0026	[7:0]	PLLCFG	RW	PLL Control configuration [7:6]: Loop Filter Resistor selection 00: 39.5k 01:30.2k **(Default)** 10:25.7k 11:15.6k [5]: PLL power down enable 1: power down 0: normal [4]: current source selection 0: internal current source **(Default)** 1: bandgap current source [3:0]: PLL ref_clk-divider Always divide ref_clk to 3MHz. 0000: 3MHz 0001: 6MHz 0010: 9MHz : 0111: 24MHz : 1111: 48MHz	0x47
0x0027	[7:0]	OUTPORTCONTROL	RW	[7]: ITU-601 Enable {[0],[6:4]}: Data Format Selector 0000: NTSC 0001: PAL 0010: YUV422 **(CbYCrY)** 0011: YUV422 (**YcbYCr)** 0100: RGB565 0101: RGB555 0110: RGB444 0111: ITU656 progressive 1000: P2I 1001: RAW_Domain **(OMUX)** 1010: RAW_Domain **(LSC)** 1011: RAW_Domain **(BPC / Denoise)** 1100: RAW_Domain **(OTP BPC output)** 1101: RAW_Domain **(BLO)** 1110: cvbs_out 1111: video tg_out [3]: Format Selector 0: CbCr non-swap 1: CbCr swap **(Refer to ColorType)** [2]: 8-bit data on 10-bit bus's format 0: Close to MSB 1: Close to LSB [1]: PCLK uses 36MHz	0x00
0x0028	[7:0]	CKMUL	RW	Test Image Control [7]: Enable Test image. **(='1')** Use Sensor Hsync / Vsync [6]: Enable Test Image **('1')** Use Internal Clock to Generate Timing [5:4]: Reserved [3:0]: Test Pattern Selection	0x00
0x0029	[7:0]	CCIR656_Ctrl	RW	[7]: CCIR656 enable 0: Disable 1: Enable [6:0]: Reserved	0x00

Address	Byte	Register name	Type	Description	Default (Hex)
0x002A	[7:0]	PLL1CFG	RW	PLL Control configuration: [7:6]: CP current selection 00: 10uA 01: 20uA 10: 30uA **(Default)** 11: 40uA [5:0]: PLL feedback-divider fvco = 6*(post_divider+1) fvco 010101: 132MHz : 010001: 108MHz : 001101: 84MHz Valid range: 01 0101 ~ 00 1101	0x91
0x002B	[7:0]	CK2CFG	RW	Reserved	0x00
0x002C	[3:0]	PLL2CFG	RW	[3:2]: ramp pwr consumption [1]: 0: divider 2 for 36MHz 1: divider 4 for 36MHz [0]: 0: divider 2 for 54MHz 1: divider 4 for 54MHz	0x00
0x002E	[4:0]	IOCNTR3	RW	Ios Control Configuration [4]: Direction of SDO [3]: Direction of SCK, SCS [2]: Direction of strobe pad [1]: Direction of sync pad [0]: Direction of TRIG pad	0x1D
0x002F	[7:0]	RESERVED	-	Reserved	0x00

11.4. Boot / IRS function control registers [0x0030 – 0x003F]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0030	[7:0]	BOOT_REF1	RO	IO strap pad value [7:6]: FLK [5]: overlay [4]: bw [3]: i2cid [2]: mirror [1]: flip [0]: boot	-
0x0031	[4:0]	BOOT_REF2	RO	[4]: use_eeprom [3:0]: DF	-
0x0032	[3:0]	BOOT_CTRL	RW	Boot function control [3]: enable bw [2]: force_clr boot function [1]: turn on rolling shutter location [0]: sensor function determine 0: by register 1: by pad	0x00
0x0033	[7] [5:3] [1:0]	CRC_FLAG	RW	[7]: WO, clear bit[4] [5]: insist turn on overlay even [4]=1 [4]: RO, CRC error flag of reading overlay content [3]: WO, clear bit[0] [1]: insist auto-trigger even [0]=1 [0]: RO, CRC error flag of reading initial setting	0x11
0x0034	[5:0]	LEDIRS_CTRL	RW	LED / IRS function control [5]: IRS0,1 output invert [4]: strobe output invert [3]: IRSI input invert [2]: enable BW_LED [1]: enable IRS output [0]: enable strobe output	0x00
0x0035	[7:0]	LED_HY_PERIOD	RW	[7:0]: LED hysteresis period	0x00
0x0036	[7:0]	IRS_PERIOD	RW	[7:0]: IRS period	0x00
0x0037	[2:0]	RESERVED	RW	Reserved	-
0x0038	[7:0]	RESERVED	RW	Reserved	-
0x0039	[7:0]	RESERVED	RW	Reserved	-
0x003A	[2:0]	RESERVED	RW	Reserved	-
0x003B	[7:0]	RESERVED	RW	Reserved	-
0x003C	[2:0]	RESERVED	RW	Reserved	-
0x003D	[7:0]	RESERVED	RW	Reserved	-
0x003E	[7:0]	RESERVED	RW	Reserved	-
0x003F	[7:0]	RESERVED	RW	Reserved	-

11.5. Black level control registers [0x0040 – 0x004F]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0040	[7:0]	BLCTGT	CMU_RW	Black level target [7:0]: Maximum of 255 ticks **(1LSB = 1ADC)**	0x20
0x0041	[7:0]	RESERVED	-	Reserved	-
0x0042	[3:0]	RESERVED	-	Reserved	-
0x0043	[7:0]	RESERVED	-	Reserved	-
0x0044	[6:0]	RESERVED	-	Reserved	-
0x0045	[7:0]	RESERVED	-	Reserved	-
0x0046	[7:0]	RESERVED	-	Reserved	-
0x0047	[1:0]	RESERVED	-	Reserved	-
0x0048	[7:0]	RESERVED	-	Reserved	-
0x0049	[7:0]	RESERVED	-	Reserved	-
0x004A	[7:0]	RESERVED	-	Reserved	-
0x004B	[7:0]	RESERVED	-	Reserved	-
0x004C	[7:0]	RESERVED	-	Reserved	-
0x004D	[6:0]	RESERVED	-	Reserved	-
0x004E	[7:0]	RESERVED	-	Reserved	-
0x004F	[6:0]	RESERVED	-	Reserved	-

11.6. Arbitrary readout window control registers [0x0050 – 0x0057]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0050	[1:0]	AnaWinVStart_1	RW	[1:0]: Y start point high byte	0x00
0x0051	[7:0]	AnaWinVStart_0	RW	[7:0]: Y start point low byte	0x1E
0x0052	[1:0]	AnaWinVEnd_1	RW	[1:0]: Y end point high byte	0x02
0x0053	[7:0]	AnaWinVEnd_0	RW	[7:0]: Y end point low byte	0x05
0x0054	[1:0]	AnaWinHStart_1	RW	[1:0]: X start point high byte	0x00
0x0055	[7:0]	AnaWinHStart_0	RW	[7:0]: X start point low byte	0x28
0x0056	[1:0]	AnaWinHEnd_1	RW	[1:0]: X end point high byte	0x02
0x0057	[7:0]	AnaWinHEnd_0	RW	[7:0]: X end point low byte	0xAF

11.7. Sensor control registers [0x007A – 0x007B]

Address	Byte	Register name	Type	Description	Default (Hex)
0x007A	[7:0]	TOTALROW_H	RO	[7:0] Total ROW time **(w.r.t ADCK)** High bytes	0x00
0x007B	[7:0]	TOTALROW_L	RO	[7:0] Total ROW time **(w.r.t ADCK)** Low bytes	0x00

11.8. ISP control registers [0x0100 – 0x0126]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0100	[7:0]	CMU_AE	WO	Command Update for RDCFG**(0x0006)**, VREAD**(0x000D)**, HREAD**(0x000E)**, IMGCFG**(0x000F)**, BLNKRH**(0x0010)**, BLNKRL**(0x0011)**, INTGH**(0x0015)**, INTGL**(0x0016)**, AGAIN**(0x0018)**, DGAIN**(0x001D)**, BLCTGT**(0x0040)**	0xFF
0x0101	[7:0]	CMU_AWB	WO	Command Update	0xFF
0x0105	[7:0]	ISPID	RO	ISP ID **(Features added, version of ISP used)**	0x01
0x0120	[7:0]	ISPCtrl_byte1	CMU_RW	ISP function control byte1 [7]: Reserved [6]: AE IIR function disable 0: IIR Enable 1: IIR Disable [5]: AE weight mode enable 0: OFF 1: ON [4]: Hue control bit 0: OFF 1: ON [3]: AE Adjust IIR function disable 0: IIR Enable 1: IIR Disable [2]: Gamma function control bit 0: OFF 1: ON [1]: Raw data offset before AWB 0: OFF 1: ON [0]: Anti-flicker reference frequency 0: 50Hz 1: 60Hz	0x37
0x0121	[7:0]	ISPCtrl_byte2	CMU_RW	ISP function control byte2 [7]: Auto black level subtraction function 0: OFF 1: ON [6]: Alpha control mode with MinBV mode 0: OFF 1: ON [5] : Hue-Sin signal bit 0: plus 1: minus [4]: Hue-Cos signal bit 0 : plus 1 : minus [3]: Indication collection white pixel for AWB statistics 0: OFF 1: ON [2]: Reserved [1]: AE near saturation mode 0: OFF 1: ON [0]: Scale up near saturation data for AE statistics. 0: 4x 1: 8x	0x81

Address	Byte	Register name	Type	Description	Default (Hex)
0x0122	[7:0]	RAWCtrlByte1	CMU_RW	[7]: Full Mode 0: Binning Mode 1: Full Frame Mode [6]: Lens shading compensation **(LSC)** Function 0: OFF 1: ON [5]: Bayer denoise function 0: OFF 1: ON [4]: g1g2_same_curve [3]: Simple BPC enable 0: OFF 1: ON [2]: Gr / Gb common adjustment 0: OFF 1: ON [1]: Manual black level offset **(BLO)** function 0: OFF 1: ON [0]: Bad pixel correction **(BPC)** function 0: OFF 1: ON	0x73
0x0123	[7:0]	RAWCtrlByte2	CMU_RW	[7]: bpc_ratio_auto_mode [6]: sel_de_pulse_enhance_mask [5]: BNB_AWB_EN 0: No AWB gain for noise model 1: Enable AWB gain for noise model [4]: BPC_CIF_bound [3:0]: maskTH	0xCC
0x0124	[7:0]	CCM_Ctrl_byte	CMU_RW	[7]: Sigh bit for normal light color temperature threshold 0: plus 1: minus [6]: Sigh bit for A light color temperature threshold 0: plus 1: minus [5]: Gamma update option 0: update always 1: keep gamma [4]: LSC g1g2 same curve enable 0: OFF 1: ON [3]: NA [2]: CTE Weight Gurantee option 0: Disable 1: Enable [1]: AWB Color Temperature Estimation 0: Disable 1: Enable [0]: AE adjust mode enable 0: Disable 1: Enable	0xDE

Address	Byte	Register name	Type	Description	Default (Hex)
0x0125	[7:0]	YUVCtrl_byte1	CMU_RW	[7]: Contrast function 0: OFF 1: ON [6]: Brightness function 0: OFF 1: ON [5]: Scaling function 0: OFF 1: ON [4]: Windowing function 0: OFF 1: ON [3]: Y denoise function 0: OFF 1: ON [2]: UV denoise function 0: OFF 1: ON [1]: Edge enhancement function 0: OFF 1: ON [0]: Fade to black **(F2B)** function 0: OFF 1: ON	0xFD
0x0126	[7:5] [2]	YUVCtrl_byte2	CMU_RW	[7]: Edge enhancement debug mode enable 0: Disable 1: Enable [6]: Fade to black control according to AE not near converged state strategy 0: Enable 1: Disable [5]: UV gray function 0: OFF 1: ON [2]: Contrast reference Y mean of AE 0: OFF 1: ON	0x70

11.9. Bad pixel correction registers [0x01E4 – 0x01E6]

Address	Byte	Register name	Type	Description	Default (Hex)
0x01E4	[5:0]	Denoise_iStrength	RW	[5:0]: Bayer denoise strength **(0~32)**	0x18
0x01E5	[5:0]	Denoise_iStrength_Alpha	RW	[5:0]: Bayer denoise strength Alpha control	0x20
0x01E6	[5:0]	Denoise_iStrength_Alpha_ODEL	RW	[5:0]: Bayer denoise strength outdoor Alpha control	0x04

11.10. Lens shading correction registers [0x0220 – 0x0252]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0220	[7:0]	Coef_Sign	RW	Coefficient Sign [7]: COE_B_X1_sign [6]: COE_Gb_X1_sign [5]: COE_Gr_X1_sign [4]: COE_R_X1_sign [3]: COE_B_X0_sign [2]: COE_Gb_X0_sign [1]: COE_Gr_X0_sign [0]: COE_R_X0_sign	0x00
0x0221	[7:0]	COE_R_X2	RW	[7:0]: COE_R_X2	0xB0
0x0222	[7:0]	COE_R_X1	RW	[7:0]: COE_R_X1	0x00
0x0223	[7:0]	COE_R_X0	RW	[7:0]: COE_R_X0	0x80
0x0224	[7:0]	COE_GB_X2	RW	[7:0]: COE_GB_X2	0x8E
0x0225	[7:0]	COE_GB_X1	RW	[7:0]: COE_GB_X1	0x00
0x0226	[7:0]	COE_GB_X0	RW	[7:0]: COE_GB_X0	0x80
0x0227	[7:0]	COE_GR_X2	RW	[7:0]: COE_GR_X2	0x8E
0x0228	[7:0]	COE_GR_X1	RW	[7:0]: COE_GR_X1	0x00
0x0229	[7:0]	COE_GR_X0	RW	[7:0]: COE_GR_X0	0x80
0x022A	[7:0]	COE_B_X2	RW	[7:0]: COE_B_X2	0x8A
0x022B	[7:0]	COE_B_X1	RW	[7:0]: COE_B_X1	0x00
0x022C	[7:0]	COE_B_X0	RW	[7:0]: COE_B_X0	0x88
0x022D	[4:0]	Shift_R_X2	RW	[4:0]: Shift_R_X2	0x13
0x022E	[4:0]	Shift_R_X1	RW	[4:0]: Shift_R_X1	0x0B
0x022F	[4:0]	Shift_GB_X2	RW	[4:0]: Shift_GB_X2	0x13
0x0230	[4:0]	Shift_GB_X1	RW	[4:0]: Shift_GB_X1	0x0B
0x0231	[4:0]	Shift_GR_X2	RW	[4:0]: Shift_GR_X2	0x13
0x0232	[4:0]	Shift_GR_X1	RW	[4:0]: Shift_GR_X1	0x0B
0x0233	[4:0]	Shift_B_X2	RW	[4:0]: Shift_B_X2	0x13
0x0234	[4:0]	Shift_B_X1	RW	[4:0]: Shift_B_X1	0x0B
0x0235	[7:0]	R_CX_LB	RW	[7:0]: R_Center_X low byte	0x6C
0x0236	[7:0]	R_CX_HB	RW	[7:0]: R_Center_X high byte	0x01
0x0237	[7:0]	Gb_CX_LB	RW	[7:0]: Gb_Center_X low byte	0x6C
0x0238	[7:0]	Gb_CX_HB	RW	[7:0]: Gb_Center_X high byte	0x01
0x0239	[7:0]	Gr_CX_LB	RW	[7:0]: Gr_Center_X low byte	0x6C
0x023A	[7:0]	Gr_CX_HB	RW	[7:0]: Gr_Center_X high byte	0x01
0x023B	[7:0]	B_CX_LB	RW	[7:0]: B_Center_X low byte	0x6C
0x023C	[7:0]	B_CX_HB	RW	[7:0]: B_Center_X high byte	0x01
0x023D	[7:0]	R_CY_LB	RW	[7:0]: R_Center_Y low byte	0x14
0x023E	[7:0]	R_CY_HB	RW	[7:0]: R_Center_Y high byte	0x01
0x023F	[7:0]	Gb_CY_LB	RW	[7:0]: Gb_Center_Y low byte	0x14
0x0240	[7:0]	Gb_CY_HB	RW	[7:0]: Gb_Center_Y high byte	0x01
0x0241	[7:0]	Gr_CY_LB	RW	[7:0]: Gr_Center_Y low byte	0x14
0x0242	[7:0]	Gr_CY_HB	RW	[7:0]: Gr_Center_Y high byte	0x01
0x0243	[7:0]	B_CY_LB	RW	[7:0]: B_Center_Y low byte	0x14
0x0244	[7:0]	B_CY_HB	RW	[7:0]: B_Center_Y high byte	0x01
0x0251	[7:0]	LSC	RW	[7:5]: NA [4:0]: LSC_ALPLA	0x0E
0x0252	[7:0]	LSC_ALPHA	RW	[7:5]: NA [4:0]: LSC_ALPLA	0x00

11.11. Gamma correction registers [0x0280 – 0x02A0]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0280	[7:0]	GAMMA1	RW	[7:0]: Gamma value for 0-XREF1	0x0D
0x0282	[7:0]	GAMMA2	RW	[7:0]: Gamma value for XREF1-XREF2	0x1A
0x0284	[7:0]	GAMMA3	RW	[7:0]: Gamma value for XREF2-XREF3	0x30
0x0286	[7:0]	GAMMA4	RW	[7:0]: Gamma value for XREF3-XREF4	0x53
0x0288	[7:0]	GAMMA5	RW	[7:0]: Gamma value for XREF4-XREF5	0x62
0x028A	[7:0]	GAMMA6	RW	[7:0]: Gamma value for XREF5-XREF6	0x6E
0x028C	[7:0]	GAMMA7	RW	[7:0]: Gamma value for XREF6-XREF7	0x7A
0x028E	[7:0]	GAMMA8	RW	[7:0]: Gamma value for XREF7-XREF8	0x83
0x0290	[7:0]	GAMMA9	RW	[7:0]: Gamma value for XREF8-XREF9	0x8B
0x0292	[7:0]	GAMMA10	RW	[7:0]: Gamma value for XREF9-XREF10	0x92
0x0294	[7:0]	GAMMA11	RW	[7:0]: Gamma value for XREF10-XREF11	0x9D
0x0296	[7:0]	GAMMA12	RW	[7:0]: Gamma value for XREF11-XREF12	0xA8
0x0298	[7:0]	GAMMA13	RW	[7:0]: Gamma value for XREF12-XREF13	0xBC
0x029A	[7:0]	GAMMA14	RW	[7:0]: Gamma value for XREF13-XREF14	0xCF
0x029C	[7:0]	GAMMA15	RW	[7:0]: Gamma value for XREF14-XREF15	0xE2
0x029E	[7:0]	GAMMASLOP	RW	[7:0]: Slope value for XREF15-255	0x2A
0x02A0	[3:0]	GAM by Alpha	RW	[3:0]: GAM by MinBV Alpha	0x02

11.12. Overlay content registers [0x02B0 – 0x02BD]

Address	Byte	Register name	Type	Description	Default (Hex)
0x02B0	[7] [0]	SF_O_Ctrl	CMU_RW	[7]: SPI status during the OVL updated [0]: Enable update OVL sram from external Flash	0x00
0x02B8	[7:0]	OVL1_Adr_hb	RW	[7:0]: Indicated start address to access external Flash for OVL1	0x02
0x02B9	[7:0]	OVL1_Adr_mb	RW	[7:0]: Indicated start address to access external Flash for OVL1	0x00
0x02BA	[7:0]	OVL1_Adr_lb	RW	[7:0]: Indicated start address to access external Flash for OVL1	0x00
0x02BB	[7:0]	OVL2_Adr_hb	RW	[7:0]: Indicated start address to access external Flash for OVL2	0x02
0x02BC	[7:0]	OVL2_Adr_mb	RW	[7:0]: Indicated start address to access external Flash for OVL2	0x10
0x02BD	[7:0]	OVL2_Adr_lb	RW	[7:0]: Indicated start address to access external Flash for OVL2	0x00

11.13. Color correction matrix registers [0x02C0 – 0x0307]

Address	Byte	Register name	Type	Description	Default (Hex)
0x02C0	[7:0]	NormCCM00_LB	RW	[7:0]: Normal Matrix00 coefficient low byte	0x7D
0x02C1	[1:0]	NormCCM00_HB	RW	[1:0]: Normal Matrix00 coefficient high byte	0x01
0x02C2	[7:0]	NormCCM01_LB	RW	[7:0]: Normal Matrix01 coefficient low byte	0x84
0x02C3	[2:0]	NormCCM01_HB	RW	[2:0]: Normal Matrix01 coefficient high byte	0x07
0x02C4	[7:0]	NormCCM02_LB	RW	[7:0]: Normal Matrix02 coefficient low byte	0xFF
0x02C5	[2:0]	NormCCM02_HB	RW	[2:0]: Normal Matrix02 coefficient high byte	0x07
0x02C6	[7:0]	NormCCM10_LB	RW	[7:0]: Normal Matrix10 coefficient low byte	0xC2
0x02C7	[2:0]	NormCCM10_HB	RW	[2:0]: Normal Matrix10 coefficient high byte	0x07
0x02C8	[7:0]	NormCCM11_LB	RW	[7:0]: Normal Matrix11 coefficient low byte	0x90
0x02C9	[1:0]	NormCCM11_HB	RW	[1:0]: Normal Matrix11 coefficient high byte	0x01
0x02CA	[7:0]	NormCCM12_LB	RW	[7:0]: Normal Matrix12 coefficient low byte	0xAE
0x02CB	[2:0]	NormCCM12_HB	RW	[2:0]: Normal Matrix12 coefficient high byte	0x07
0x02CC	[7:0]	NormCCM20_LB	RW	[7:0]: Normal Matrix20 coefficient low byte	0xFC
0x02CD	[2:0]	NormCCM20_HB	RW	[2:0]: Normal Matrix20 coefficient high byte	0x07
0x02CE	[7:0]	NormCCM21_LB	RW	[7:0]: Normal Matrix21 coefficient low byte	0x57
0x02CF	[2:0]	NormCCM21_HB	RW	[2:0]: Normal Matrix21 coefficient high byte	0x07
0x02D0	[7:0]	NormCCM22_LB	RW	[7:0]: Normal Matrix22 coefficient low byte	0xAD
0x02D1	[1:0]	NormCCM22_HB	RW	[1:0]: Normal Matrix22 coefficient high byte	0x01
0x02E0	[3:0]	CCM by Alpha	RW	[3:0]: CCM by Alpha	0x04
0x02F0	[7:0]	CCM_RDIFF_R_LB	RW	[7:0]: Difference between Normal and A light on Matrix00 coefficient low byte	0xB2
0x02F1	[2:0]	CCM_RDIFF_R _HB	RW	[2:0]: Difference between Normal and A light on Matrix00 coefficient high byte	0x07
0x02F2	[7:0]	CCM_RDIFF_G _LB	RW	[7:0]: Difference between Normal and A light on Matrix01 coefficient low byte	0xB1
0x02F3	[2:0]	CCM_RDIFF_G _HB	RW	[2:0]: Difference between Normal and A light on Matrix01 coefficient high byte	0x00
0x02F4	[7:0]	CCM_RDIFF_B_LB	RW	[7:0]: Difference between Normal and A light on Matrix02 coefficient low byte	0x9D
0x02F5	[2:0]	CCM_RDIFF_B _HB	RW	[2:0]: Difference between Normal and A light on Matrix02 coefficient high byte	0x07
0x02F6	[7:0]	CCM_GDIFF_R_LB	RW	[7:0]: Difference between Normal and A light on Matrix10 coefficient low byte	0xD8
0x02F7	[2:0]	CCM_GDIFF_R_HB	RW	[2:0]: Difference between Normal and A light on Matrix10 coefficient high byte	0x07
0x02F8	[7:0]	CCM_GDIFF_G_LB	RW	[7:0]: Difference between Normal and A light on Matrix11 coefficient low byte	0xD7
0x02F9	[2:0]	CCM_GDIFF_G _HB	RW	[2:0]: Difference between Normal and A light on Matrix11 coefficient high byte	0x07
0x02FA	[7:0]	CCM_GDIFF_B_LB	RW	[7:0]: Difference between Normal and A light on Matrix12 coefficient low byte	0x51
0x02FB	[2:0]	CCM_GDIFF_B_HB	RW	[2:0]: Difference between Normal and A light on Matrix12 coefficient high byte	0x00
0x02FC	[7:0]	CCM_BDIFF_R _LB	RW	[7:0]: Difference between Normal and A light on Matrix20 coefficient low byte	0x9C
0x02FD	[2:0]	CCM_BDIFF_R_HB	RW	[2:0]: Difference between Normal and A light on Matrix20 coefficient high byte	0x07
0x02FE	[7:0]	CCM_BDIFF_G_LB	RW	[7:0]: Difference between Normal and A light on Matrix21 coefficient low byte	0x95
0x02FF	[2:0]	CCM_BDIFF_G _HB	RW	[2:0]: Difference between Normal and A light on Matrix21 coefficient high byte	0x07
0x0300	[7:0]	CCM_BDIFF_B _LB	RW	[7:0]: Difference between Normal and A light on Matrix22 coefficient low byte	0xCF
0x0301	[2:0]	CCM_BDIFF_B _HB	RW	[2:0]: Difference between Normal and A light on Matrix22 coefficient high byte	0x00
0x0302	[6:0]	Normal_CCM_03	RW	Normal Matrix03 coefficient.	0x00
0x0303	[6:0]	Normal_CCM_13	RW	Normal Matrix13 coefficient	0x00
0x0304	[6:0]	Normal_CCM_23	RW	Normal Matrix23 coefficient	0x00

Address	Byte	Register name	Type	Description	Default (Hex)
0x0305	[6:0]	CCM_RDIFF_C	RW	Difference between Normal and A light on Matrix03 coefficient	0x00
0x0306	[6:0]	CCM_GDIFF_C	RW	Difference between Normal and A light on Matrix13 coefficient	0x00
0x0307	[6:0]	CCM_BDIFF_C	RW	Difference between Normal and A light on Matrix23 coefficient	0x00

11.14. AWB digital channel gain registers [0x032D – 0x0332]

Address	Byte	Register name	Type	Description	Default (Hex)
0x032D	[7:0]	GainRed_LB	RW	[7:0]: AWB channel gain for red low byte	0x70
0x032E	[1:0]	GainRed_HB	RW	[1:0]: AWB channel gain for red high byte	0x01
0x032F	[7:0]	GainGreen_LB	RW	[7:0]: AWB channel gain for green low byte	0x00
0x0330	[1:0]	GainGreen_HB	RW	[1:0]: AWB channel gain for green high byte	0x01
0x0331	[7:0]	GainBlue_LB	RW	[7:0]: AWB channel gain for blue low byte	0x70
0x0332	[1:0]	GainBlue_HB	RW	[1:0]: AWB channel gain for blue high byte	0x01

11.15. AWB detection registers [0x0340 – 0x034C]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0340	[7:0]	WPDCTTH	RW	[7:0]: WPD Threshold	0x50
0x0343	[7:0]	R_CT1_WBG	RW	[7:0]: Red gain for color temperature 1	0x1A
0x0344	[7:0]	B_CT1_WBG	RW	[7:0]: Blue gain for color temperature 1	0x80
0x0345	[7:0]	R_CT2_WBG	RW	[7:0]: Red gain for color temperature 2	0x43
0x0346	[7:0]	B_CT2_WBG	RW	[7:0]: Blue gain for color temperature 2	0x7D
0x0347	[7:0]	R_CT3_WBG	RW	[7:0]: Red gain for color temperature 3	0x50
0x0348	[7:0]	B_CT3_WBG	RW	[7:0]: Blue gain for color temperature 3	0x6A
0x0349	[7:0]	R_CT4_WBG	RW	[7:0]: Red gain for color temperature 4	0x5D
0x034A	[7:0]	B_CT4_WBG	RW	[7:0]: Blue gain for color temperature 4	0x57
0x034B	[7:0]	R_CT5_WBG	RW	[7:0]: Red gain for color temperature 5	0x60
0x034C	[7:0]	B_CT5_WBG	RW	[7:0]: Blue gain for color temperature 5	0x4D

11.16. Auto exposure configuration registers [0x0380 – 0x0395]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0380	[1:0]	AEWBCFG	RW	AE and AWB Control [1]: AWB enable 0: bypass 1: ON [0]: AE enable 0: bypass 1: ON	0xFF
0x0381	[7:0]	AETARGU	RW	[7:0]: AE target mean upper bound	0x48
0x0382	[7:0]	AETARGL	RW	[7:0]: AE target mean lower bound	0x30
0x0383	[7:0]	AEMINM	RW	[7:0]: AE minimum mean setting	0x0A
0x038E	[7:0]	AETARGM	RW	[7:0]: AE target mean value	0x3C
0x038F	[7:0]	AEMXEXH	RW	[7:0]: AE maximum exposure setting high byte (**MSB)**	0x02
0x0390	[7:0]	AEMXEXL	RW	[7:0]: AE maximum exposure setting low byte **(LSB)**	0x34
0x0391	[7:0]	AEMNEX	RW	[7:0]: AE minimum exposure setting	0x01
0x0392	[7:0]	AEMXAG	RW	[7:0]: AE setting of maximum analog coarse gain	0x03
0x0393	[7:0]	AEMXDG	RW	[7:0]: AE setting of maximum digital gain	0x80
0x0394	[7:0]	AEMNDG	RW	[7:0]: AE setting of minimum digital gain	0x40
0x0395	[7:0]	AESKIP	RW	AE setting of PG-FM skip count [7:4]: AWB_pg_skipcnt [3:0]: AE_pg_skipcnt	0x23

11.17. Frame rate priority mode registers [0x0398 – 0x03B1]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0398	[7:0]	AEMXEXTH1H	RW	[7:0]: Maximum exposure TH1 high Byte	0x02
0x0399	[7:0]	AEMXEXTH1L	RW	[7:0]: Maximum exposure TH1 low Byte	0x34
0x039A	[7:0]	AEMXEXTH2H	RW	[7:0]: Maximum exposure TH2 high Byte	0x02
0x039B	[7:0]	AEMXEXTH2L	RW	[7:0]: Maximum exposure TH2 low Byte	0xC1
0x039C	[7:0]	AEMXEXTH3H	RW	[7:0]: Maximum exposure TH3 high Byte	0x03
0x039D	[7:0]	AEMXEXTH3L	RW	[7:0]: Maximum exposure TH3 low Byte	0x4E
0x039E	[7:0]	AEMXEXTH4H	RW	[7:0]: Maximum exposure TH4 high Byte	0x04
0x039F	[7:0]	AEMXEXTH4L	RW	[7:0]: Maximum exposure TH4 low Byte	0x68
0x03A0	[7:0]	AEMXEXTH5H	RW	[7:0]: Maximum exposure TH5 high Byte	0x05
0x03A1	[7:0]	AEMXEXTH5L	RW	[7:0]: Maximum exposure TH5 low Byte	0x82
0x03A2	[7:0]	AEMXEXTH6H	RW	[7:0]: Maximum exposure TH6 high Byte	0x06
0x03A3	[7:0]	AEMXEXTH6L	RW	[7:0]: Maximum exposure TH6 low Byte	0x9C
0x03A4	[7:0]	AEMXEXTH7H	RW	[7:0]: Maximum exposure TH7 high Byte	0x08
0x03A5	[7:0]	AEMXEXTH7L	RW	[7:0]: Maximum exposure TH7 low Byte	0xD0
0x03A6	[7:0]	AETGTH12	RW	[7:0]: TG TH12	0x18
0x03A7	[7:0]	AETGTH23	RW	[7:0]: TG TH23	0x1C
0x03A8	[7:0]	AETGTH34	RW	[7:0]: TG TH34	0x20
0x03A9	[7:0]	AETGTH45	RW	[7:0]: TG TH45	0x24
0x03AA	[7:0]	AETGTH56	RW	[7:0]: TG TH56	0x28
0x03AB	[7:0]	AETGTH67	RW	[7:0]: TG TH67	0x30
0x03AC	[7:0]	AETGTH76	RW	[7:0]: TG TH76	0x24
0x03AD	[7:0]	AETGTH65	RW	[7:0]: TG TH65	0x21
0x03AE	[7:0]	AETGTH54	RW	[7:0]: TG TH54	0x1C
0x03AF	[7:0]	AETGTH43	RW	[7:0]: TG TH43	0x18
0x03B0	[7:0]	AETGTH32	RW	[7:0]: TG TH32	0x17
0x03B1	[7:0]	AETGTH21	RW	[7:0]: TG TH21	0x13

11.18. AE statistics registers [0x03B3 – 0x03ED]

Address	Byte	Register name	Type	Description	Default (Hex)
0x03B3	[7:0]	AECntORG_V_LB	RW	[7:0]: AE origin windowing point for vertical low byte	0x10
0x03B4	[7:0]	AECntORG_V_HB	RW	[7:0]: AE origin windowing point for vertical high byte	0x00
0x03B5	[7:0]	AECntORG_H_LB	RW	[7:0]: AE origin windowing point for horizontal low byte	0x10
0x03B6	[7:0]	AECntORG_H_HB	RW	[7:0]: AE origin windowing point for horizontal high byte	0x00
0x03B7	[7:0]	AECntST_V_LB	RW	[7:0]: AE windowing step for vertical low byte	0x70
0x03B8	[7:0]	AECntST_V_HB	RW	[7:0]: AE windowing step for vertical high byte	0x00
0x03B9	[7:0]	AECntST_H_LB	RW	[7:0]: AE windowing step for horizontal low byte	0x90
0x03BA	[7:0]	AECntST_H_HB	RW	[7:0]: AE windowing step for horizontal high byte	0x00
0x03BB	[7:0]	BVWinEnArray_LB	RW	BV window enable bit **(Low byte)** [7]: Win24 [6]: Win23 [5]: Win22 [4]: Win21 [3]: Win14 [2]: Win13 [1]: Win12 [0]: Win11	0xFF
0x03BC	[7:0]	BVWinEnArray_MB	RW	BV window enable bit **(High byte)** [7]: Win44 [6]: Win43 [5]: Win42 [4]: Win41 [3]: Win34 [2]: Win33 [1]: Win32 [0]: Win31	0xFF
0x03E0	[6:4] [2:0]	WinWeight_1_12	RW	BV window weight 100: 12.5% 000: 25% 001: 50% 010: 75% 011: 100% [6:4]: WinWeight_1_2 [2:0]: WinWeight_1_1	0x10
0x03E1	[6:4] [2:0]	WinWeight_1_34	RW	BV window weight 100: 12.5% 000: 25% 001: 50% 010: 75% 011: 100% [6:4]: WinWeight_1_4 [2:0]: WinWeight_1_3	0x01
0x03E4	[6:4] [2:0]	WinWeight_2_12	RW	BV window weight 100: 12.5% 000: 25% 001: 50% 010: 75% 011: 100% [6:4]: WinWeight_2_2 [2:0]: WinWeight_2_1	0x21

Address	Byte	Register name	Type	Description	Default (Hex)
0x03E5	[6:4] [2:0]	WinWeight_2_34	RW	BV window weight 100: 12.5% 000: 25% 001: 50% 010: 75% 011: 100% [6:4]: WinWeight_2_4 [2:0]: WinWeight_2_3	0x12
0x03E8	[6:4] [2:0]	WinWeight_3_12	RW	BV window weight 100: 12.5% 000: 25% 001: 50% 010: 75% 011: 100% [6:4]: WinWeight_3_2 [2:0]: WinWeight_3_1	0x32
0x03E9	[6:4] [2:0]	WinWeight_3_34	RW	BV window weight 100: 12.5% 000: 25% 001: 50% 010: 75% 011: 100% [6:4]: WinWeight_3_4 [2:0]: WinWeight_3_3	0x23
0x03EC	[6:4] [2:0]	WinWeight_4_12	RW	BV window weight 100: 12.5% 000: 25% 001: 50% 010: 75% 011: 100% [6:4]: WinWeight_4_2 [2:0]: WinWeight_4_1	0x21
0x03ED	[6:4] [2:0]]	WinWeight_4_34	RW	BV window weight 100: 12.5% 000: 25% 001: 50% 010: 75% 011: 100% [6:4]: WinWeight_4_4 [2:0]: WinWeight_4_3	0x12

11.19. Auto BLC control registers (RGB domain) [0x0430 – 0x0437]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0430	[7:0]	ABLC_Def	RW	[7:0]: ABLC default value	0x08
0x0431	[7:0]	ABLC_MAX	RW	[7:0]: ABLC maximum value	0x34
0x0432	[7:0]	ABLC_Tol	RW	[7:0]: ABLC tolerance offset	0x0C
0x0433	[7:0]	ABLC_LCHB	RW	[7:0]: ABLC lower point count for high Byte	0x04
0x0435	[7:0]	ABLC_UCHB	RW	[7:0]: ABLC upper point count for high Byte	0x08
0x0437	[7:0]	ABLC_REF	RO	Reserved	0x00

11.20. Alpha control registers [0x0450 – 0x0479]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0450	[7:0]	Alpha1_Coef	RW	[7:0]: Piecewise coefficient for Alpha1	0xFF
0x0451	[7:0]	Alpha2_Coef	RW	[7:0]: Piecewise coefficient for Alpha2	0xD0
0x0452	[7:0]	Alpha3_Coef	RW	[7:0]: Piecewise coefficient for Alpha3	0xB8
0x0453	[7:0]	Alpha4_Coef	RW	[7:0]: Piecewise coefficient for Alpha4	0x88
0x0454	[7:0]	Alpha5_Coef	RW	[7:0]: Piecewise coefficient for Alpha5	0x00
0x0455	[7:0]	Alpha6_Coef	RW	[7:0]: Piecewise coefficient for Alpha6	0x00
0x0456	[7:0]	Alpha7_Coef	RW	[7:0]: Piecewise coefficient for Alpha7	0x00
0x0457	[7:0]	Alpha8_Coef	RW	[7:0]: Piecewise coefficient for Alpha8	0x00
0x0458	[7:0]	ODEL1_Coef	RW	[7:0]: Outdoor Piecewise coefficient	0x80
0x0459	[3:0]	ODEL0_Coef	RW	[3:0]: Outdoor Piecewise coefficient 0000: ODEL1 - 0; 0001: ODEL1 - 8'd8; 0010: ODEL1 - 8'd16; 0011: ODEL1 - 8'd32; 0100: ODEL1 - 8'd64; 0101: ODEL1 - 8'd128;	0x03
0x045A	[1:0]	CT1_Coef_HB	RW	[1:0]: Normal Color Temperature **(CT)** threshold high byte The sign bit at 0x0124[7]	0x00
0x045B	[7:0]	CT1_Coef_LB	RW	[7:0]: Normal Color Temperature **(CT)** threshold low byte	0x50
0x045C	[1:0]	CT0_Coef_HB	RW	[1:0]: A light Color Temperature **(CT)** threshold high byte The sign bit at 0x0124[6]	0x00
0x045D	[7:0]	CT0_Coef_LB	RW	[7:0]: A light Color Temperature **(CT)** threshold low byte	0x90
0x0470	[7:0]	Current_Alpha	RO	[7:0]: Current Alpha Value	0x00
0x0471	[7:0]	Current_Alpha_ODEL	RO	[7:0]: Current Alpha_ODEL Value	0x00
0x0472	[7:0]	Current_Alpha_CT	RO	[7:0]: Current Alpha_CT Value	0x00
0x0478	[7:0]	M_Alpha_TG	RW	[7:0]: 0: Auto-Alpha_TG Else: Manual Alpha_TG	0x00
0x0479	[7:0]	Current_Alpha_TG	RO	[7:0]: Current Alpha_TG Value	0x00

11.21. Color space transform / UV adjustment registers [0x0480 – 0x0488]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0480	[7:0]	SatB	RW	[7:0]: Cb Saturation	0x58
0x0481	[7:0]	SatB_Alpha	RW	[7:0]: Cb Saturation for MinBV Alpha control	0x06
0x0482	[7:0]	SatB_Alpha_ODEL	RW	[7:0]: Saturation control for outdoor Cb Alpha control	0x08
0x0486	[7:0]	HueSIN	RW	[7:0]: Hue Sin control parameter or Image scene for Cb **(If Image Scene = 1 && Hue Enable = 0)**	0x00
0x0487	[7:0]	HueCOS	RW	[7:0]: Hue Cos control parameter or Image scene for Cr **(If Image Scene = 1 && Hue Enable = 0)**	0xFF
0x0488	[5:4] [1:0]	Image_Scene	RW	[5:4]: Gain limited 00: OFF 01: all function 10: w/o Rmax/Bmax Compensation 11: maximum function only [1]: Image XOR effective enable 0: bypass 1: ON [0]: Image scene enable 0: bypass 1: ON	0x30

11.22. Contrast / Brightness registers [0x04B0 – 0x04C3]

Address	Byte	Register name	Type	Description	Default (Hex)
0x04B0	[7:0]	Contrast_M	RW	[7:0]: Contrast stage 2 slope Range: 0~FF	0x50
0x04B1	[7:0]	Contrast_M_Alpha	RW	[7:0]: Contrast stage 2 slope for MinBV Alpha control Range: 0~FF±7F*2	0x85
0x04B3	[6:0]	Contrast_Q	RW	[6:0]: Contrast center adjustment **(Contrast center means input equal to output)** Range: 0~7F	0x00
0x04B4	[6:0]	Contrast_Q_Alpha	RW	[6:0]: Contrast center adjustment for MinBV Alpha control Range: 0~7F±7F	0x00
0x04B6	[6:0]	Contrast_N	RW	[6:0]: Contrast stage 1 and stage 4 slope Range: 0~40	0x30
0x04B7	[7:0]	Contrast_N_Alpha	RW	Reserved	0x00
0x04B9	[6:0]	Contrast_P	RW	[6:0]: Contrast stage 3 offset Range: 0~40	0x10
0x04BA	[7:0]	Contrast_P_Alpha	RW	Reserved	0x00
0x04BC	[4:0]	Contrast_Gain	RW	[4:0]: Contrast Gain **(>=1)**	0x00
0x04BD	[7:0]	Y_MEAN	RW	[7:0]: Y mean for contrast center **(Contrast center means input equal to output)**	0x3C
0x04BE	[4:0]	Contrast_Gain_Alpha	RW	[4:0]: Contrast Gain with alpha **(>=1)**	0x00
0x04C0	[7:0]	BN_BRIGHTNESS	RW	[7:0]: Y brightness strength	0x00
0x04C1	[7:0]	Reserved	-	Reserved	-
0x04C2	[6:0]	YUV_Control_BYTE	RW	[6:5]: YUV_top/P2I vsync out sync with 00: hr+hr, 01: hr+hf, 10: hf+hr, 11: hf+hf [4]: bli ccm enable [3]: P2I enable [2:0]: special_effect_sel 000: no special effect 001: emboss 010: sketch 011: solarize mid-tone 100: solarize all 101: manual y value **(0x4C3[7:0])**	0x00
0x04C3	[7:0]	manual_y	RW	[7:0] manual y value for special_effect_sel **(0x4C2[2:0])**=3'h5	0x00

11.23. Flicker detection registers [0x0540 – 0x0549]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0540	[7:0]	Flicker_step_60hz_H	RW	[7:0]: AE flicker step setting for 60Hz high byte	0x00
0x0541	[7:0]	Flicker_step_60hz_L	RW	[7:0]: AE flicker step setting for 60Hz low byte	0x8D
0x0542	[7:0]	Flicker_step_50hz_H	RW	[7:0]: AE flicker step setting for 50Hz high byte	0x00
0x0543	[7:0]	Flicker_step_50hz_L	RW	[7:0]: AE flicker step setting for 50Hz low byte	0xA9
0x0544	[7:0]	Snapshot_fstep_60hz_H	RW	[7:0]: AE flicker step setting high byte for 60Hz for capture mode	0x00
0x0545	[7:0]	Snapshot_fstep_60hz_L	RW	[7:0]: AE flicker step setting low byte for 60Hz for capture mode	0x00
0x0546	[7:0]	Snapshot_fstep_50hz_H	RW	[7:0]: AE flicker step setting high byte for 50Hz for capture mode	0x00
0x0547	[7:0]	Snapshot_fstep_50hz_L	RW	[7:0]: AE flicker step setting low byte for 50Hz for capture mode	0x00
0x0548	[3:0]	Flicker_step_60hz_F	RW	[3:0]: 4-bit fraction of AE flicker step setting for 60Hz	0x00
0x0549	[3:0]	Flicker_step_50hz_F	RW	[3:0]: 4-bit fraction of AE flicker step setting for 50Hz	0x00

11.24. Auto exposure new registers [0x054C – 0x054F]

Address	Byte	Register name	Type	Description	Default (Hex)
0x054C	[3:0]	AESRINTG_CTRL	RW	[4]: Analog fine gain calculation enable [3]: sub_row_INTG threshold select 0: use flicker step as threshold 1: use 0x54D~54E as threshold [2]: force to allow extraN/16 row, which extraN is 0x550[7:4] **(Default is not allow 1/16 row)** [1:0]: mode control 00: normal **(no sub_row_INTG)** 01: sub_row_INTG switch mode 10: full sub_row_INTG mode	0x00
0x054D	[7:0]	AESRINTG_TH_H	RW	[7:0]: sub_row_INTG threshold **(H)**	0x00
0x054E	[7:0]	AESRINTG_TH_L	RW	[7:0]: sub_row_INTG threshold **(L)**	0x00
0x054F	[7:0]	AESRINTG_FLK_TH	RW	Flicker step hysteresis [7:0]: u1.7	0x80

11.25. YUV de-noise registers [0x0580 – 0x0582]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0580	[3:0]	Blur_Weight	RW	[3:0]: Y denoise strength Range: 0~15	0x04
0x0581	[3:0]	Blur_Weight_alpha	RW	[3:0]: Y denoise strength for total gain Alpha control Range: 0~15	0x0F
0x0582	[3:0]	Blur_Weight_alpha_ODEL	RW	[3:0]: Y denoise strength for Outdoor Alpha Control Range: 0~15	0x04

11.26. Sharpness registers [0x05A1]

Address	Byte	Register name	Type	Description	Default (Hex)
0x05A1	[7:0]	EE_SHARP_EDGE	RW	Sharpness strength	0x0A

11.27. Windowing / Scaling registers [0x05E0 – 0x05EC]

Address	Byte	Register name	Type	Description	Default (Hex)
0x05E0	[7:0]	YUV_SCX_LB	RW	[7:0]: Scaling X size low byte	0xC7
0x05E1	[7:0]	YUV_SCX_HB	RW	[7:0]: Scaling X size high byte	0x71
0x05E2	[7:0]	YUV_SCY_LB	RW	[7:0]: Scaling Y size low byte	0x00
0x05E3	[7:0]	YUV_SCY_HB	RW	[7:0]: Scaling Y size high byte	0x80
0x05E4	[7:0]	YUV_WINX_ST_LB	RW	[7:0]: Windowing X start pixel low byte	0x04
0x05E5	[1:0]	YUV_WINX_ST_HB	RW	[1:0]: Windowing X start pixel high byte	0x00
0x05E6	[7:0]	YUV_WINX_ED_LB	RW	[7:0]: Windowing X end pixel low byte	0x83
0x05E7	[1:0]	YUV_WINX_ED_HB	RW	[1:0]: Windowing X end pixel high byte	0x02
0x05E8	[7:0]	YUV_WINY_ST_LB	RW	[7:0]: Windowing Y start pixel low byte	0x04
0x05E9	[1:0]	YUV_WINY_ST_HB	RW	[1:0]: Windowing Y start pixel high byte	0x00
0x05EA	[7:0]	YUV_WINY_ED_LB	RW	[7:0]: Windowing Y end pixel low byte	0xE3
0x05EB	[1:0]	YUV_WINY_ED_HB	RW	[1:0]: Windowing Y end pixel high byte	0x01
0x05EC	[7:0]	Scaler_Control_BYTE	RW	[7]: TV-Encoder color bars en On/off EIA **(NTSC mode)** and EBU **(PAL mode)** color bars [6:4]: scaler offset adjust scaler sram read start timing, start to read at scaler offset*16 clocks [3]: hsc method 0: horizontal linear interpolation 1: horizontal cubic**(x4)** & linear interpolation [2:0]: scaler mode 000: NTSC active 640x480 → 720x480 001: NTSC active 714x536 → 720x480 010: NTSC active 720x536 → 720x480 011: PAL active 706x530 → 720x576 100: PAL active 720x530 → 720x576	0x00

11.28. Overlay control registers [0x0A00 – 0x0A0F]

Address	Byte	Register name	Type	Description	Default (Hex)
0x0A00	[7:0]	{LTOP_OPAQUE, LBOT_OPAQUE, LTOP_BUF_IDX, LBOT_BUF_IDX, OSD_BUF_MODE, LTOP_EN, LBOT _EN}	RW	[7]: Top layer force opaque [6]: Bottom layer force opaque 0: alpha is decided by color palette 1: alpha is 8 [5]: Top layer buffer index 0: read BUF0 1: read BUF1 [4]: Bottom layer buffer index 0: read BUF0 1: read BUF1 [3:2]: OSD_BUF_MODE 4K-buffer **(2048x16)**, BUF1/BUF2 size 0: 4K/0K, 1:3K/1K, 2:2K/2K [1]: l2_overlay_en [0]: l1_overlay_en	0x00
0x0A01	[3:0]	{LTOP_SCALE_MODE, LBOT_SCALE_MODE}	RW	[3:2]: Top layer OSD scale mode [1:0]: Bottom layer OSD scale mode 00: Hx1/Vx1, 2'd1: Hx2/Vx1, 10: Hx1/Vx2, 2'd3: Hx2/Vx2	0x00
0x0A02	[0]	LBOT_X_OFFSET_SIGN	RW	[0]: Bottom layer Overlay X offset sign bit	0x00
0x0A03	[7:0]	LBOT_X_OFFSET	RW	[7:0]: Bottom layer Overlay X offset value	0x00
0x0A04	[0]	LBOT_Y_OFFSET_SIGN	RW	[0]: Bottom layer Overlay Y offset sign bit	0x00
0x0A05	[7:0]	LBOT_Y_OFFSET	RW	[7:0]: Bottom layer Overlay Y offset value	0x00
0x0A06	[0]	LTOP_X_OFFSET_SIGN	RW	[0]: Top layer Overlay X offset sign bit	0x00
0x0A07	[7:0]	LTOP_X_OFFSET	RW	[7:0]:Top layer Overlay X offset value	0x00
0x0A08	[0]	LTOP_Y_OFFSET_SIGN	RW	[0]: Top layer Overlay Y offset sign bit	0x00
0x0A09	[7:0]	LTOP_Y_OFFSET	RW	[7:0]: Top layer Overlay Y offset value	0x00
0x0A0A	[7:0]	LBOT_BLINK_PERIOD	RW	[7:0]: Bottom layer blink period 8'd0: always display 8'dt: switch overlay on/off every 10*t frames	0x00
0x0A0B	[7:0]	LTOP_BLINK_PERIOD	RW	[7:0]: Top layer blink period 8'd0: always display 8'dt: switch overlay on/off every 10*t frames	0x00
0x0A0C	[1:0]	LBOT_TIMEOUT_H	RW	[1:0] Bottom layer timeout high byte 10'd0: always display, 10'dt: turn off overlay after 10*t frames	0x00
0x0A0D	[7:0]	LBOT_TIMEOUT_L	RW	[7:0]: Bottom layer timeout low byte 10'd0: always display, 10'dt: turn off overlay after 10*t frames	0x00
0x0A0E	[1:0]	LTOP_TIMEOUT_H	RW	[1:0] Top layer timeout high byte 10'd0: always display, 10'dt: turn off overlay after 10*t frames	0x00
0x0A0F	[7:0]	LTOP_TIMEOUT_L	RW	[7:0] Top layer timeout low byte 10'd0: always display, 10'dt: turn off overlay after 10*t frames	0x00

12. Electrical Specification

12.1. Absolute maximum ratings

Parameter		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
Ambient storage temperature		T_{ST}	-40	-	85	°C
Operating temperature **(Junction temperature)**		T_{OP}	-30	-	85	°C
Stable image temperature(1) **(Junction temperature)**		T_{SI}	0	-	60	°C
Analog supply voltage		V_{DD-A_MAX}	-0.3	-	4.0	V
Digital supply voltage		V_{DD-D_MAX}	-0.3	-	2.0	V
IO supply voltage		V_{DD-IO_MAX}	-0.3	-	4.0	V
DC input voltage		DC_{IN}	-0.3	-	V_{DD-IO} + 0.3	V
ESD rating	Human Body Model	ESD	-	2000	-	V
	Machine Model		-	200	-	V

Note: (1) The sensor will produce stable images within the temperature range and within the operating limits of the electrical specification. The image quality is not guaranteed when operating the sensor beyond the stable image temperature specification.

(2) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

12.2. Operating voltages

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Analog supply voltage	V_{DD-A}	3.0	3.3	3.6	V
Digital supply voltage	V_{DD-D}	1.35	1.5	1.65	V
IO supply voltage	V_{DD-IO}	1.7	1.8	3.6	V

12.3. DC characteristics

(The power consumptions are measured by using internal test pattern. (Set 0x0028=0x87))

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Current Consumption						
Active current **(Parallel)**	$I_{DD-AVDD}$	Bypass Internal LDO Mode, Video, full resolution @60FPS, V_{DD-A} = 3.3V,V_{DD-D} = 1.5V, V_{DD-IO} = 3.3V	-	18	29	mA
	$I_{DD-DVDD}$		-	44	66	mA
	$I_{DD-IOVDD}$		-	17	27	mA
Active current **(Parallel)**	$I_{DD-AVDD}$	Internal LDO Mode Video, full resolution @60FPS V_{DD-A} = 3.3V, V_{DD-LDO} = 3.3V V_{DD-IO} = 3.3V	-	19	31	mA
	I_{DD-LDO}		-	45	72	mA
	$I_{DD-IOVDD}$		-	17	27	mA
Active current **(CVBS)**	$I_{DD-AVDD}$	Bypass Internal LDO Mode Video, full resolution @NTSC0 V_{DD-A} = 3.3V,V_{DD-D} = 1.5V V_{DD-IO} = 3.3V	-	55	88	mA
	$I_{DD-DVDD}$		-	42	67	mA
	$I_{DD-IOVDD}$		-	3	6	mA
Active current **(CVBS)**	$I_{DD-AVDD}$	Internal LDO Mode Video, full resolution @NTSC0 V_{DD-A} = 3.3V, V_{DD-LDO} = 3.3V V_{DD-IO} = 3.3V	-	55	88	mA
	I_{DD-LDO}		-	45	72	mA
	$I_{DD-IOVDD}$		-	3	6	mA
Standby current	$I_{DD-PWDN}$	PWDN pin initiated at 1.8V V_{DD-A} = 3.3V, V_{DD-D} = 3.3V, V_{DD-IO} = 3.3V, MCLK is provided	-	0.3	1000	µA
Digital Inputs (MCLK, SCL, PWDN)						
Input voltage low	V_{IL}	-	GND - 0.3	-	$0.3V_{DD-IO}$	V
Input voltage high	V_{IH}	-	$0.7V_{DD-IO}$	-	V_{DD-IO} + 0.3	V
Input capacitance	C_{IN}	-	-	4		pF
Digital Output						
Output voltage low	V_{OL}	-	-	-	$0.2V_{DD-IO}$	V
Output voltage high	V_{OH}	-	$0.8V_{DD-IO}$	-	-	V
Output current **IOCNTRH[6:4] & [2:0]** 000: 1x 001: 2x 010: 3x 011: 4x 100: 5x 101: 6x 110: 7x 111: 8x	I_O	C_L = 25pF	-	I_{OL} | I_{OH}	-	mA
Output capacitance	C_{OUT}	-	-	4	-	pF
Output resistance	R_{OUT}	-	-	1	-	Ω
Tri-state leakage current	I_{OZ}	-	-	-	10	µA
Digital Inputs (MCLK, SCL, PWDN)						
Input voltage low	V_{IL}	-	GND - 0.3	-	$0.3V_{DD-IO}$	V
Input voltage high	V_{IH}	-	$0.7V_{DD-IO}$	-	V_{DD-IO} + 0.3	V
Input capacitance	C_{IN}	-	-	4	-	pF

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Video DAC Electrical Characteristics (Single Ended Mode)						
DAC resolution	RES	-	-	10	-	bit
Differential non-linearity	DNL	-	-	1	-	LSB
Integral non-linearity	INL	-	-	3	-	LSB
Output pad **(IOUTP)**	R_{LOAD_P}	-	-	75	-	Ω
Unused **(IOUTN)**	R_{LOAD_N}	-	-	37.5	-	Ω
DAC reference	RSET	-	-	2.0	-	KΩ

12.4. Master clock input

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Input frequency	MCLK	Program PLL Bypass PLL	3	27	48	MHz
Input clock duty cycle	$MCLK_{DUTY}$	-	45	-	55	%

12.5. Serial bus characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Input clock frequency	F_{SCL}	-	100	-	400	kHz
Input clock period	t_{SCL}	-	2.5	-	10	µs
Input clock duty cycle	-	-	40	50	60	%
Rise time of SCL/SDA	t_{RT}	-	-	-	$0.12T_{SCL}$(1)	ns
Fall time of SCL/SDA	t_{FT}	-	-	-	$0.12T_{SCL}$(1)	ns
Start setup time	t_{HD_SU}	Write	T_{MCLK}(2)	-	-	ns
Start hold time	t_{HD_STA}	Write	$3T_{MCLK}$(2)	-	-	ns
Data hold time	t_{HD_DAT}	Write	5	-	-	ns
Data setup time	t_{SU_DAT}	Write	$3T_{MCLK}$(2)	-	-	ns
Stop setup time	t_{SU_STP}	Write	$3T_{MCLK}$(2)	-	-	ns
Stop hold time	t_{HD_STP}	Write	T_{MCLK}(2)	-	-	ns
Data hold time	t_{HD_DATR}	Read	$3T_{MCLK}$(2)	-	-	ns
Data setup time	t_{SU_DATR}	Read	T_{SCL}(1)/2-t_{HD_DATR}	-	-	ns
SDA maximum load capacitance	C_{SDA_LOAD}	-	-	-	4.2	pF
SDA pull-up resistor	R_{SDA}	-	500	-	-	Ω

Note: (1) T_{SCL} = Cycle time of SCL.
(2) T_{MCLK} = Cycle time of MCLK.

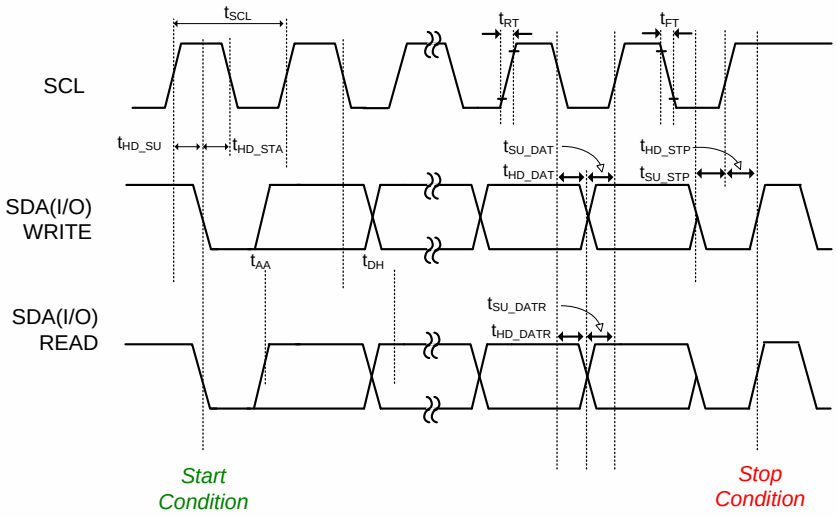


Figure 12.1: 2-Wire serial interface timing diagram

12.6. Parallel interface timing characteristics

Conditions: T_A = 25ºC, C_L = 15pF, F_{PLCKO} = 54MHz

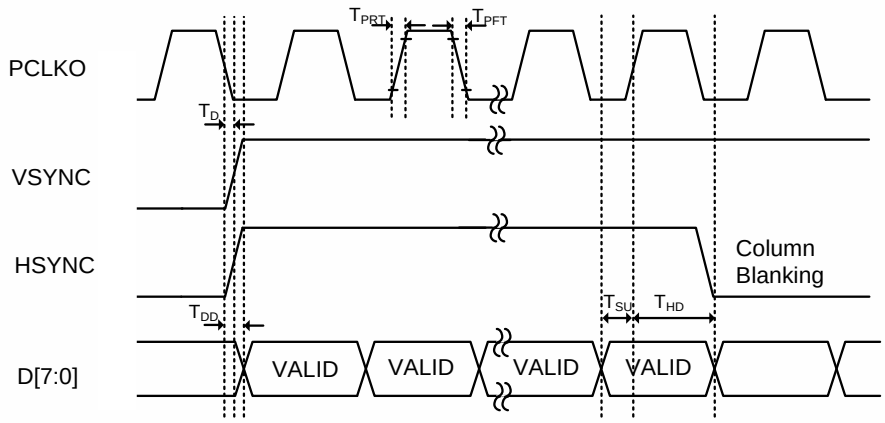


Figure 12.2: Parallel video interface timing diagram

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
PCLKO period	T_{PLCKO}	-	18.5	-	ns
PCLKO rise time	T_{PRT}	-	3.8	-	ns
PCLKO fall time	T_{PFT}	-	3.4	-	ns
PCLKO falling edge to HSYNC, VSYNC rising edge delay	T_D	-	4.6	-	ns
PCLKO falling edge to DATA transition delay	T_{DD}	-	3.2	-	ns
Data bus setup time	T_{SU}	-	6.0	-	ns
Data bus hold time	T_{HD}	-	12.5	-	ns

12.7. NTSC video timing characteristics

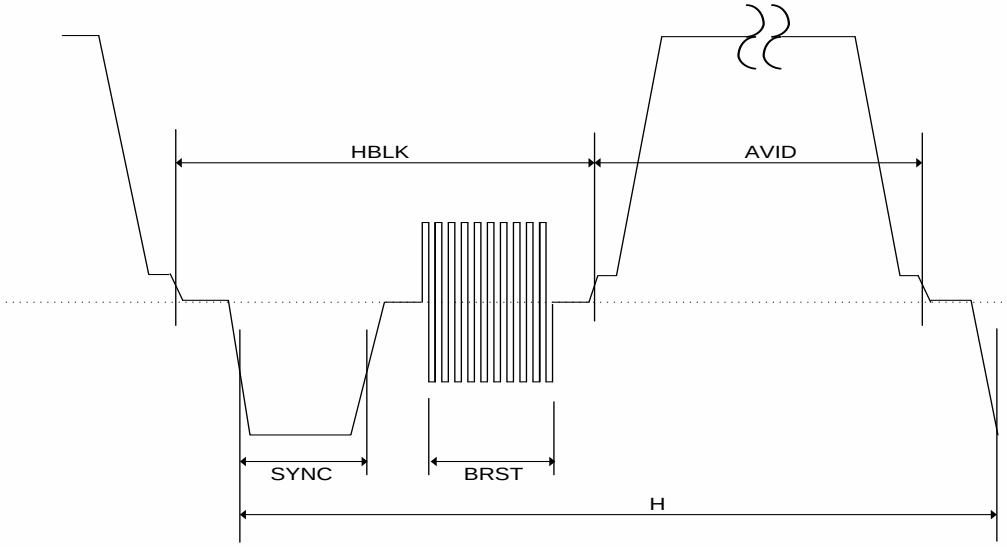


Figure 12.3: NTSC video output timing

(Conditions: T_A = 25ºC, R_{LOAD_P} = 75Ω)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Horizontal Blanking	T_{HBLK}	-	10.75	-	µs
Active Video	T_{AVID}	-	52.8	-	µs
Sync Tip	T_{SYNC}	-	4.75	-	µs
Color Burst	T_{BRST}	-	9	-	cycle
H Period	T_{HPULSE}	-	63.55	-	µs

12.8. PAL video timing characteristics

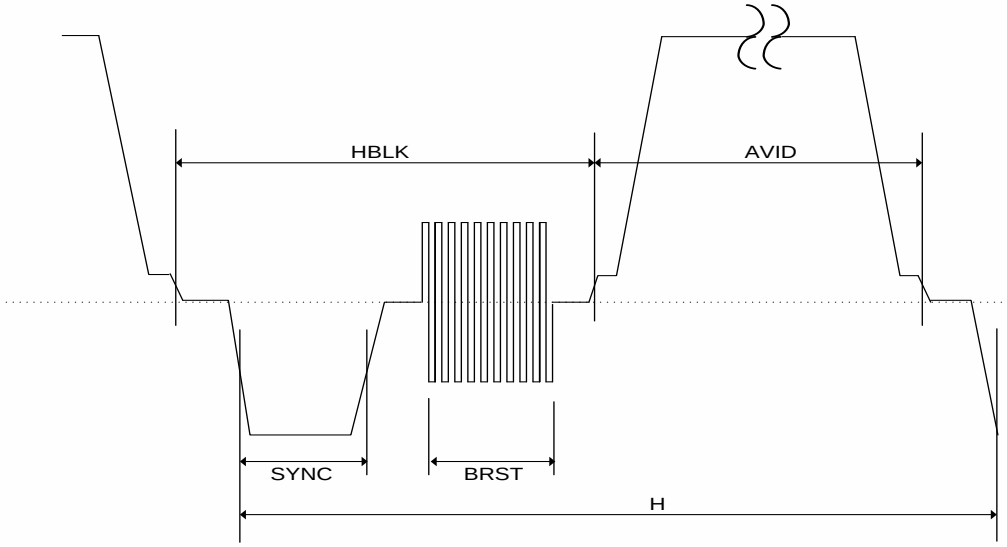


Figure 12.4: PAL video output timing

(Conditions: T_A = 25ºC, R_{LOAD_P} = 75Ω)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Horizontal Blanking	T_{HBLK}	-	11.85	-	µs
Active Video	T_{AVID}	-	52.15	-	µs
Sync Tip	T_{SYNC}	-	4.68	-	µs
Color Burst	T_{BRST}	-	2.37	-	µs
H Period	T_{HPULSE}	-	64	-	µs

13. Sensor Chief Ray Angle (CRA)

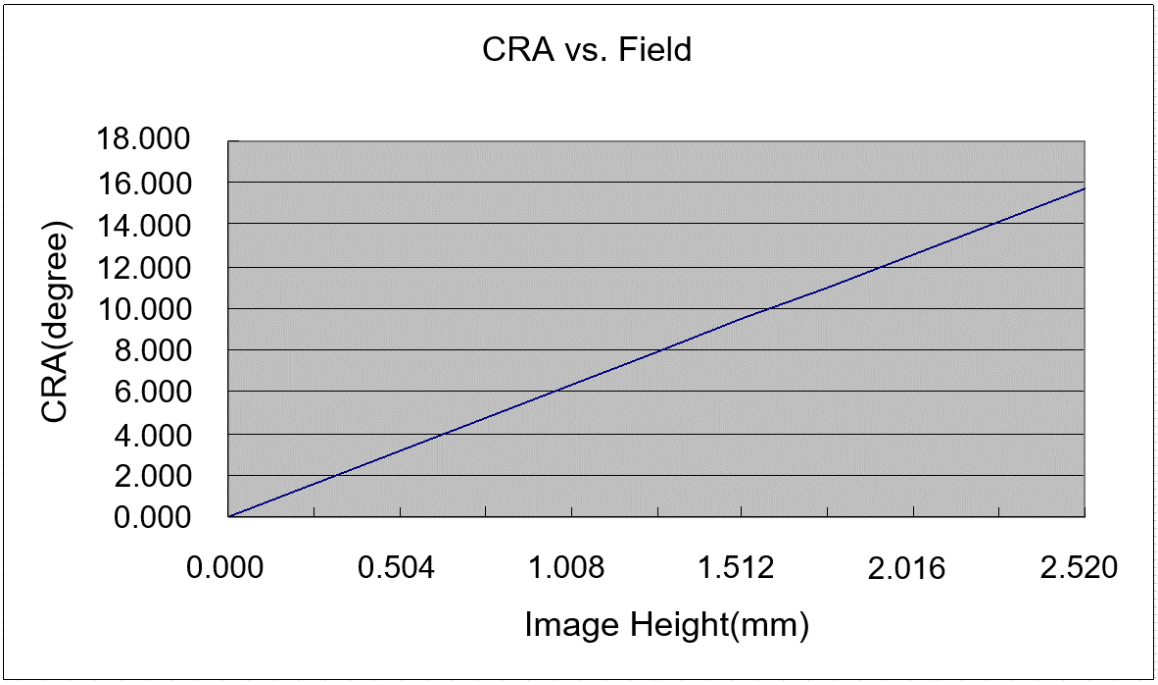


Figure 13.1: Lens CRA profile

Field (%)	Image Height (mm)	CRA (degree)
0.00	0.000	0.000
0.10	0.252	1.575
0.20	0.504	3.150
0.30	0.756	4.725
0.40	1.008	6.300
0.50	1.260	7.875
0.60	1.512	9.450
0.70	1.764	11.025
0.80	2.016	12.600
0.90	2.268	14.175
1.00	2.520	15.750

Table 13.1: CRA profile

14. Quantum Efficiency (QE)

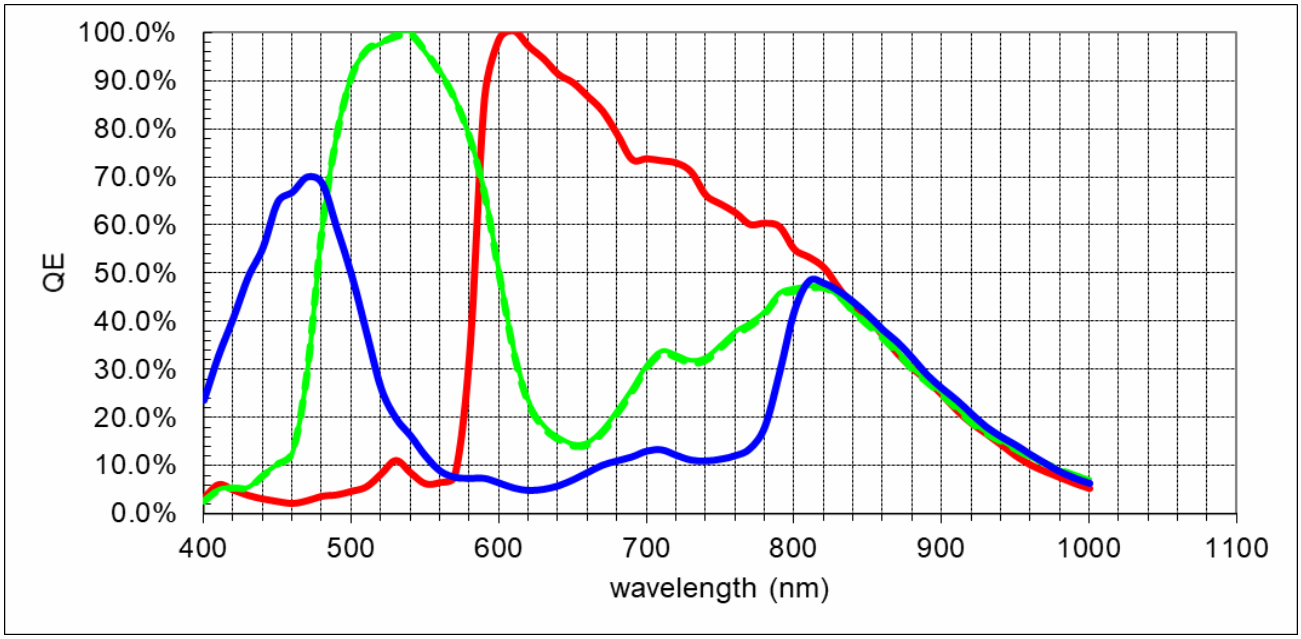


Figure 14.1: Relative QE