Himax Imaging, Ltd.

DATA SHEET

(DOC No. HM1246-AWD-DS)

HM1246-AWD

1/3.7″ Megapixel
System-on-Chip Image Sensor

Version 01 March, 2023

Himax Imaging, Ltd.

HM1246-AWD UltraSense™

1/3.7″ Megapixel System-on-Chip Image Sensor

Himax Imaging, Ltd.
http://www.himax.com.tw

March, 2023

Features

- Low power Megapixel image sensor
- UltraSense™ BSI pixel technology
- 1280 x 960 active pixel array operating up to 60FPS in 10-bit RAW mode, and 30FPS in 8-bit YCbCr mode
- Flexible horizontal and vertical window readout
- High quality ISP with automatic exposure, gain, white balance, and image quality optimization control loop
- On-chip 3Kb OTP memory with internal charge pump
- OTP, SPI or I2C memory support for sensor boot
- SPI and I2C memory programming through SIave I2C
- Embedded temperature sensor
- Dynamic overlay engine simultaneously displays two independent image layers up to 8KB
- Window and up-scalar function for digital zoom
- External frame **(FSIN)** synchronization
- Embedded data for register status, error flag, temperature value, and frame count
- Brown-out detection for supply and temperature
- Interface, logic and memory check
- LED and Iris support

Key Parameters

Sensor Parameters	Value
Pixel Array **(Full / Active)**	1416 x 976 / 1296 x 976(1)
Pixel Size and Technology	3.0μm x 3.0μm, BSI
Image Diagonal	4.8mm
Optical Format	1/3.7″
Color Filter Array	Bayer
Scan Mode	Progressive
Shutter Type	Electronic Rolling Shutter
Frame Rate **(RAW)**	10-bit, 960p 60FPS @ 85MHz 10-bit, 800p 60FPS @ 72MHz 10-bit, 720p 60FPS @ 74.25MHz
Frame Rate **(YUV)**	960p, 30FPS @ 85MHz 800p, 30FPS @ 72MHz
S/N Ratio **(Max. @1x)**	38.5 dB
Dynamic Range (1x) **(RAW)**	62 dB
Sensitivity **(Color)**	4.35 V/Lux-sec
Pixel CRA **(Max.)**	24.79°

Note: (1) Max. of 1296x976 pixels can be read out

Sensor Parameters	Value
Supply Voltage **(Typ.)**	AVDD 3.3V DVDD (LDO) 1.5V **(1.8V)** IOVDD 1.7 – 3.6V
Input Reference Clock	6 – 27MHz; 27MHz crystal option
Serial Interface	I2C, 1MHz **(Max.)**
Serial Peripheral Interface	48MHz **(Max.)**
Video Data Interface	10-bit Parallel with SYNC
Pixel Clock	96MHz **(Max.)**
Output Format	8-bit / 10-bit RAW 8-bit YCbCr 8-bit RGB565 / 555 / 444
Power Consumption **(RAW)**	10-bit, 960p 60FPS 239.5mW 10-bit, 800p 60FPS 215.7mW 10-bit, 720p 60FPS 202.8mW
Power Consumption **(YUV)**	960p 30FPS 233.5mW 800p 30FPS 208.7mW 720p 30FPS 193.1mW
Power Consumption	Shutdown 0.5 μW

Order Information

Part no.	Color option	Operating / Storage temperature	Package
HM1246-AWD	RGB	- 40 ºC to 105 ºC / - 40 ºC to 125 ºC	CSP

Revision History

March, 2023

Version	Date	Description of changes
01	2023/03/30	New setup

List of Contents

March, 2023

List of Contents

List of Figures

List of Tables

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1. Package Information

1.1. Chip Scale Package

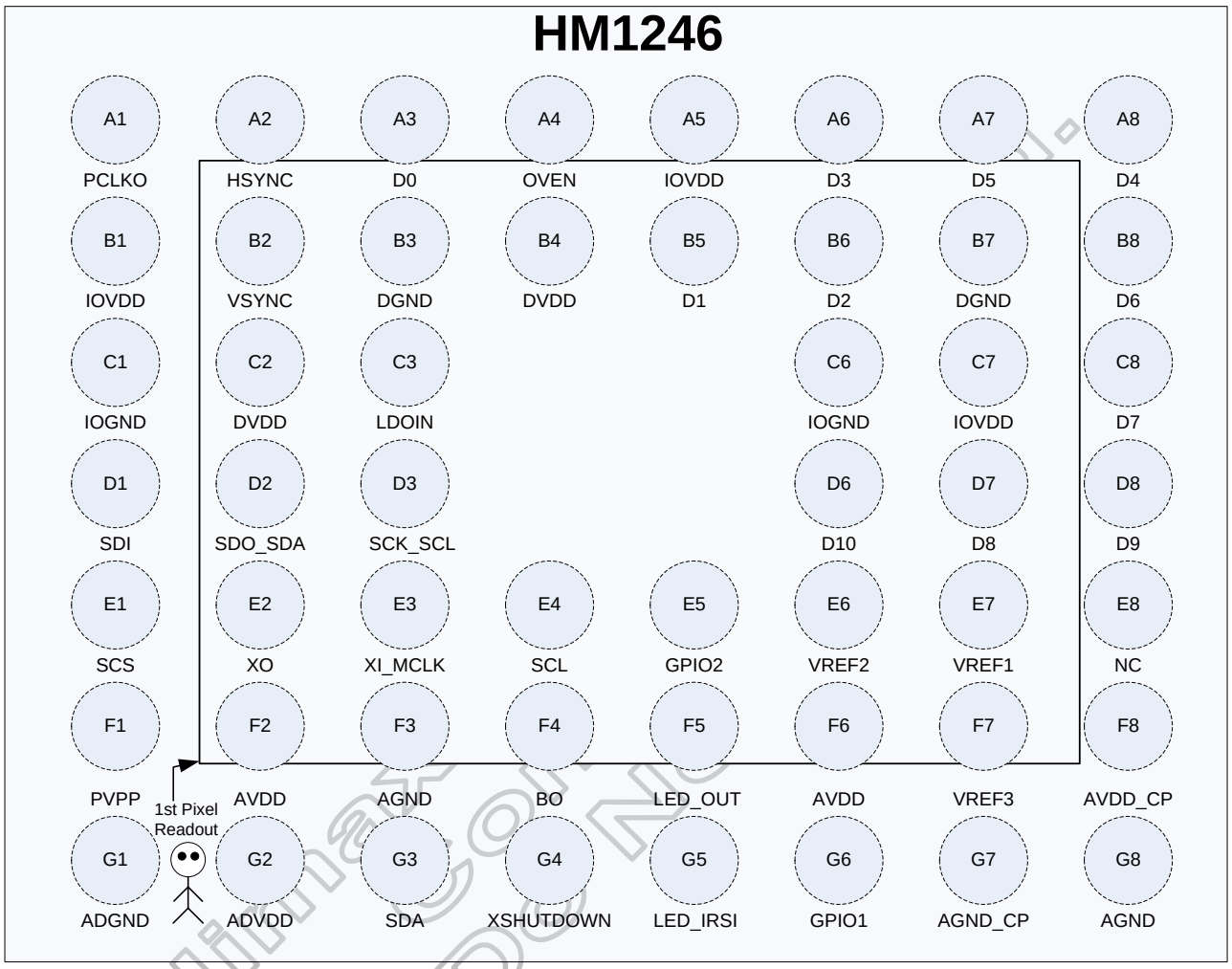


Figure 1.1: Chip Scale Package (Top view)

Pin no.	Pin name	Type	Internal PU/PD	Description
A1	PCLKO	Out	N/A	Pixel clock output.
A2	HSYNC	In/Out	Pull Down	Horizontal sync output. Boot function. FLK[1:0]={VSYNC,HSYNC}: LL: 60 Hz LH: 50 Hz HX: By register bit 0xD120[0]
A3	D0	In/Out	Pull Down	Video data output bit 0. Boot function. I2CID[1:0]={D1,D0}: LL: I2C device address=0x24 **(7-bit)** LH: I2C device address=0x25 **(7-bit)** HL: I2C device address=0x34 **(7-bit)** HH: I2C device address=0x35 **(7-bit)**
A4	OVEN	In	Pull Up	Overlay enable. L: Disable overlay engine. H: Enable overlay engine.
A5	IOVDD	Power	N/A	I/O power. **(1.7V ~ 3.6V)**
A6	D3	In/Out	Pull Down	Video data output bit 3. Boot function. MEM_CFG[1:0]={D4,D3}: LL: No external memory. LH: I2C EEPROM. HL: SPI EEPROM / FLASH. HH: Reserved.
A7	D5	In/Out	Pull Down	Video data output bit 5. Boot function. (a) I2C EEPROM: L: Support 11-bit address. **(3-bit in control byte & 8-bit in address byte)** H: Support 2-byte address. (b) SPI EEPROM / FLASH: L: Support 2-byte address. H: Support 3-byte address.
A8	D4	In/Out	Pull Down	Video data output bit 4. Boot function. MEM_CFG[1:0]={D4,D3}: LL: No external memory. LH: I2C EEPROM. HL: SPI EEPROM / FLASH. HH: Reserved.
B1	IOVDD	Power	N/A	I/O power. **(1.7V ~ 3.6V)**
B2	VSYNC	In/Out	Pull Down	Vertical sync output. Boot function. FLK[1:0]={VSYNC,HSYNC}: LL: 60 Hz. LH: 50 Hz. HX: By register bit 0xD120[0].
B3	DGND	Ground	N/A	Digital ground.
B4	DVDD	Power	N/A	Digital power. **(1.5V)**
B5	D1	In/Out	Pull Down	Video data output bit 1. Boot function. I2CID[1:0]={D1,D0} LL: I2C device address=0x24. **(7-bit)** LH: I2C device address=0x25. **(7-bit)** HL: I2C device address=0x34. **(7-bit)** HH: I2C device address=0x35. **(7-bit)**
B6	D2	Out	Pull Down	Video data output bit 2.

Pin no.	Pin name	Type	Internal PU/PD	Description
B7	DGND	Ground	N/A	Digital ground.
B8	D6	In/Out	Pull Down	Video data output bit 6. Boot function. L: Output normal image. H: Output mirrored image.
C1	IOGND	Ground	N/A	IO ground.
C2	DVDD	Power	N/A	Digital power. **(1.5V)**
C3	LDOIN	Power	N/A	Digital power for Internal LDO. **(Typ. 1.8V)** If using bypass mode, LDOIN=1.5V. Otherwise LDOIN= 1.7V~3.6V.
C6	IOGND	Ground	N/A	IO ground.
C7	IOVDD	Power	N/A	I/O power. **(1.7V ~ 3.6V)**
C8	D7	In/Out	Pull Down	Video data output bit 7. Boot function. L: Output normal image. H: Output flipped image.
D1	SDI	In	Pull Down	SPI: Data input.
D2	SDO_SDA	In/Out	Pull Down	Multifunctional I/O pin. (a) SPI: Data output. (b) I2C master: Serial data bus.
D3	SCK_SCL	Out	N/A	Multifunctional I/O pin. (a) SPI: Clock output. (b) I2C master: Serial clock output.
D6	D10	-	-	No connection.
D7	D8	In/Out	Pull Up	Video data output bit 8. Boot function. L: Boot by an external controller. H: Self-booted.
D8	D9	In/Out	Pull Down	Video data output bit 9. Boot function. L: Output color image. H: Output black & white image.
E1	SCS	Out	N/A	SPI: Chip select.
E2	XO	Out	N/A	Crystal pad. If XI_MCLK is connected to an oscillator, this pin should be left unconnected. Otherwise, this pin should be connected to the other pin of the crystal.
E3	XI_MCLK	In	N/A	Master clock input. This pin can be connected to an oscillator **(In this case, XO is left unconnected)** or connected to a crystal
E4	SCL	In	N/A	Serial clock input. **(I2C slave)**
E5	GPIO2	In/Out	Pull Down	LED_IRS: IRS0 - IR cut switch control 0.
E6	VREF2	Reference	N/A	Reference voltage.
E7	VREF1	Reference	N/A	Reference voltage.
E8	NC	-	-	No connection.
F1	PVPP	Power	N/A	Power input for OTP programming **(Normal: floating; Programming: 7.5V)** or place an external capacitor if the internal OTP pump is used.
F2	AVDD	Power	N/A	Analog power. **(3.0V ~ 3.6V)**
F3	AGND	Ground	N/A	Analog ground.
F4	BO	Out	N/A	Brown out flag signal.
F5	LED_OUT	Out	N/A	LED_IRS: LED control.
F6	AVDD	Power	N/A	Analog power. **(3.0V ~ 3.6V)**
F7	VREF3	Reference	N/A	Reference voltage.

Pin no.	Pin name	Type	Internal PU/PD	Description
F8	AVDD_CP	Power	N/A	Analog power. **(3.0V ~ 3.6V)**
G1	ADGND	Ground	N/A	Digital ground.
G2	ADVDD	Power	N/A	Digital power. **(1.5V)**
G3	SDA	In/Out	N/A	Serial data bus. **(Open Drain) (I2C slave)**
G4	XSHUTDOWN	In	Pull Down	Hardware shutdown input. **(Active low)**
G5	LED_IRSI	In	Pull Down	LED_IRS: IRSI -LED illumination sensor input.
G6	GPIO1	In/Out	Pull Down	Multifunctional IO pin. (a) LED_IRS: IRS1 - IR cut switch control 1. (b) FSIN: Frame Synchronization Input.
G7	AGND_CP	Ground	N/A	Analog ground.
G8	AGND	Ground	N/A	Analog ground.

Table 1.1: CSP pin description

2. Sensor Overview

The HM1246-AWD is a highly integrated and compact CMOS Image Sensor **(CIS)** System-on-Chip **(SOC)** with an active pixel resolution of 1296**(H)** x 976**(V)**. The sensor uses Himax Imaging's UltraSense™ Back Side Illuminated **(BSI)** pixel technology that significantly improves angular response, blooming characteristics, and low light sensitivity offering 30% higher quantum efficiency compared with Front Side Illuminated pixel.

The HM1246-AWD integrates a high quality Image Signal Processor **(ISP)** with Automatic Gain / Exposure and Automatic White Balance control loop. The ISP supports RAW processing for black level correction, lens shade compensation, defect correction and noise filtering; and a full RGB / YUV color processing pipeline for demosaicing, color correction, gamma correction, sharpening, green channel mismatch and luma / chroma noise reduction.

The HM1246-AWD supports multiple sensor initialization options using internal One Time Programmable **(OTP)** memory and external Serial Peripheral Interface **(SPI)** or I2C memory. An in-sensor programming mode allows the SPI memory to be programmed through the I2C interface. The sensor offers a high level of integration including multiple camera synchronization, On Screen Display **(OSD)**, video up scalar, temperature sensor, clock oscillator, fast locking clock generator, and embedded data detailing select sensor registers, AE/AWB statistics, and status information.

The HM1246-AWD operates up to 30 frames per second in YCbCr / RGB data format, and up to 60 frames per second in 10-bit RAW data format over a parallel data interface with video line and frame sync output. All sensor registers can be programmed using I2C interface. The sensor is offered in an ultra-compact Chip Scale Package and is rated for an ambient temperature of -40°C to 105°C operation.

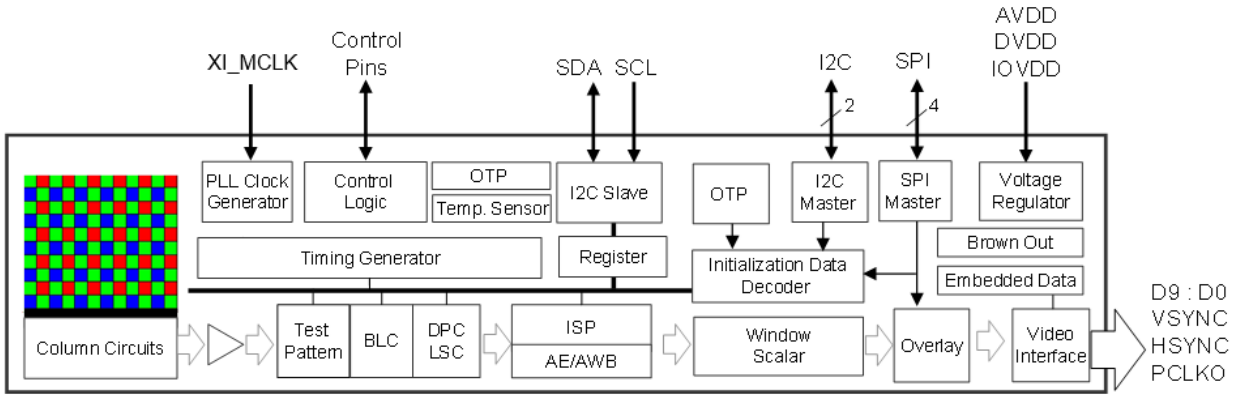


Figure 2.1: HM1246-AWD block diagram

3. Sensor Core and Function Description

3.1. Sensor array

The HM1246-AWD consists of a full pixel array of 1416 columns and 976 rows. The left 60 columns and the right 60 columns are dummy pixels. The sensor maximum active resolution is 1296 columns and 976 rows which include 8 border pixels that are used by the on-chip Image Signal Processor **(ISP)** in YUV mode, which will be cropped by the digital window block, or by an off-chip ISP in RAW mode.

The even numbered rows contain the Blue **(B)** and Green **(G_1)** pixel, and the odd numbered row contains the Red **(R)** and Green **(G_2)** pixels; the even numbered columns contain the Green **(G_2)** and Blue **(B)** pixels, and the odd column contains the Red **(R)** and Green **(G_1)** pixels. Optically black rows are used by the sensor for black level calibration. Programmable horizontal and vertical blanking time adjusts the line width and frame height, respectively.

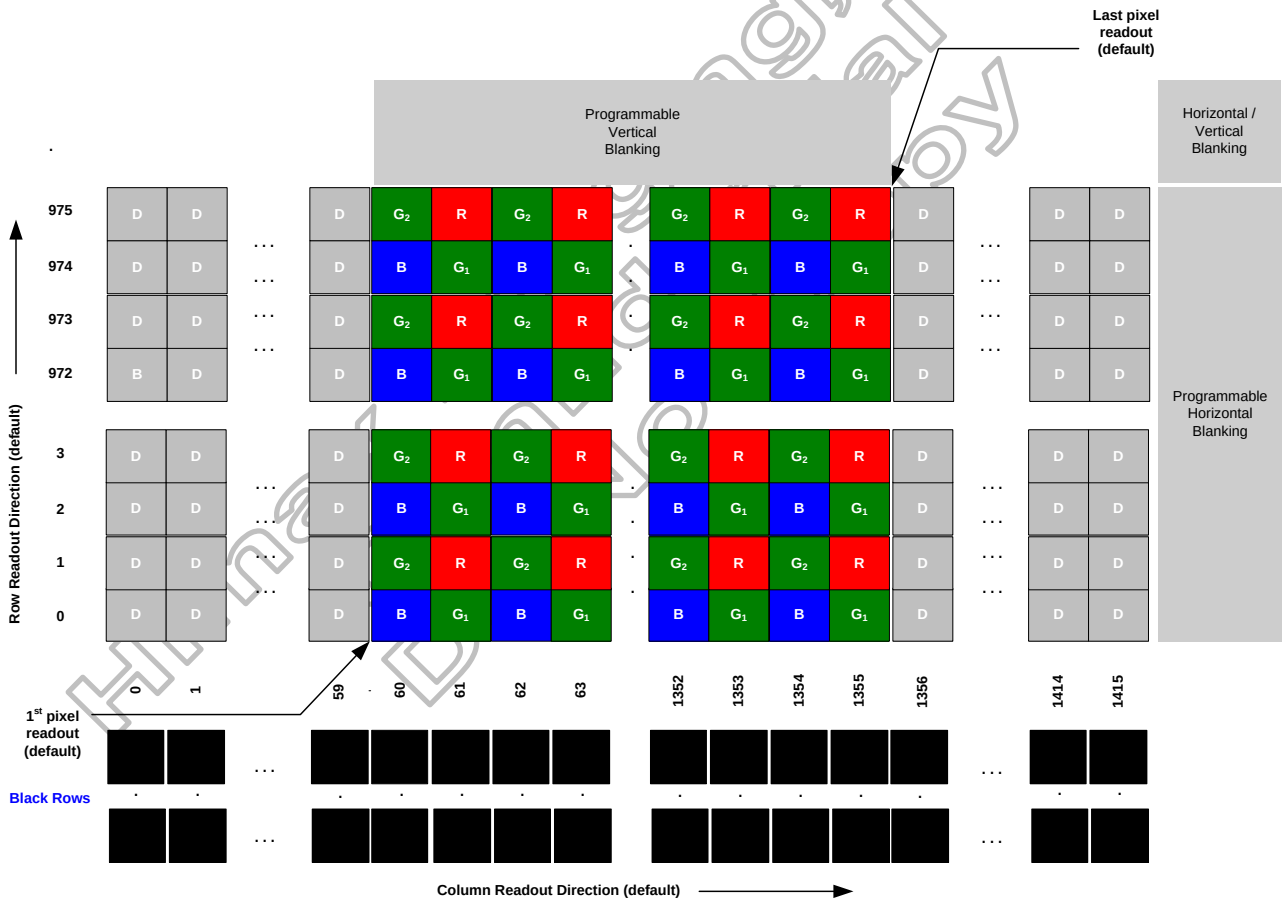


Figure 3.1: Full resolution pixel readout (Color)

3.2. Sensor window readout

The sensor window readout of HM1246-AWD has two parts. The first window is programmed by selecting the starting and ending row coordinates, and the starting and ending column coordinates within the full pixel array of 1416 x 976. The maximum window size is 1296 x 976.

The second window is used to support cropping function. By default, the 1296 x 976 window center is set to the sensor's optical center by setting the first pixel coordinate to register bits X_LA_START = 60 and register bits Y_LA_START = 0, and the last pixel to a coordinate of register bits X_LA_END = 1355 and register bits Y_LA_END = 975. For color sensor, the X_LA_START / Y_LA_START / X_ADDR_START / Y_ADDR_START should be set to an even pixel coordinate to maintain the color order.

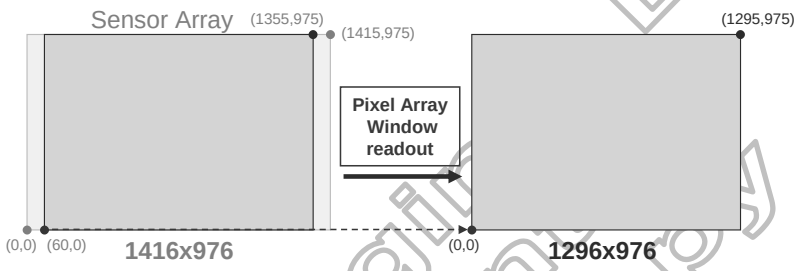


Figure 3.2: Spatial illustration of default pixel array window readout

Address	Register name	Value
0x351	X_LA_START_H	0x00
0x352	X_LA_START_L	0x3C
0x353	X_LA_END_H	0x05
0x354	X_LA_END_L	0x4B
0x355	Y_LA_START_H	0x00
0x356	Y_LA_START_L	0x00
0x357	Y_LA_END_H	0x03
0x358	Y_LA_END_L	0xCF

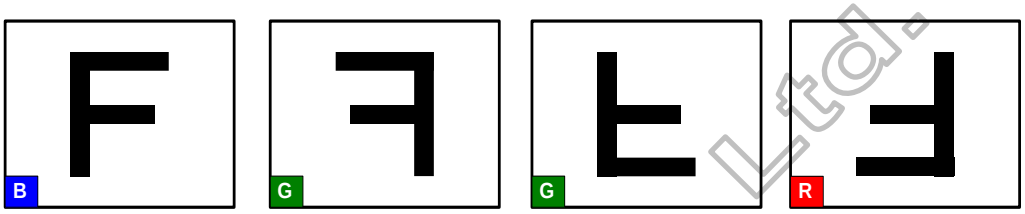
Address	Register name	Value
0x0344	X_ADDR_START_H	0x00
0x0345	X_ADDR_START_L	0x00
0x0346	Y_ADDR_START_H	0x00
0x0347	Y_ADDR_START_L	0x00
0x0348	X_ADDR_END_H	0x05
0x0349	X_ADDR_END_L	0x0F
0x034A	Y_ADDR_END_H	0x03
0x034B	Y_ADDR_END_L	0xCF

Table 3.1: Default settings of pixel array window

3.3. Horizontal and vertical mirror

The sensor readout can be mirrored in the vertical and / or horizontal direction.

- The window center will remain unchanged
- In vertical mirror **(flip)** readout mode. the rows are readout in reverse order, which will result in the appearance of the image being flipped upside down.
- In horizontal mirror readout mode, the columns are readout in reverse order, which will result in the appearance of the image being flipped along the vertical axis.
- Horizontal and vertical mirror readout can be used in all readout modes.



Default	Horizontal Mirror	Vertical Flip	V & H Mirror
0x0101[1:0] = 00	0x0101[1:0] = 01	0x0101[1:0] = 10	0x0101[1:0] = 11

Figure 3.3: Horizontal and vertical mirror readout modes

3.4. 4:2 Pixel sub-sampling and binning

Row and column sub-sampling can be used to reduce the sensor resolution while preserving the field of view.

- The HM1246-AWD sensor supports a 4:2 **(2x2)** sub-sampling
- In order to preserve the native aspect ratio of the imager, the number of rows skipped should equal the number of columns skipped.
- Enabling the binning mode averages the signals to reduce noise
- The line length and frame length should be set to 4n.

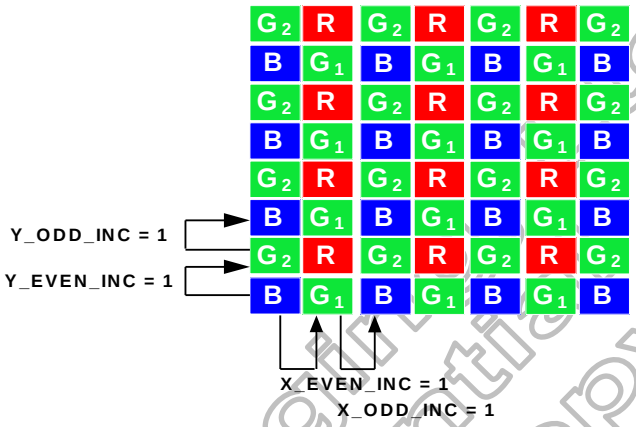


Figure 3.4: Full frame readout

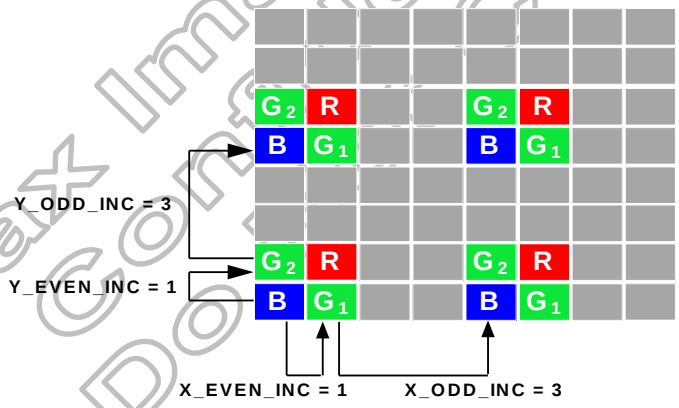


Figure 3.5: Sub-sampled readout

4. Image Signal Processor Functional Description

The sensor features an Image Signal Processor which consists of RAW data processing, RGB / YUV data processing, and automatic control loops for exposure and gain, white balance, and lowlight control. The control loop can be enabled in YUV mode **(post-color processing)** or 10-bit 30FPS RAW mode **(processed raw data)**. The ISP can be configured by the host through the serial register interface.

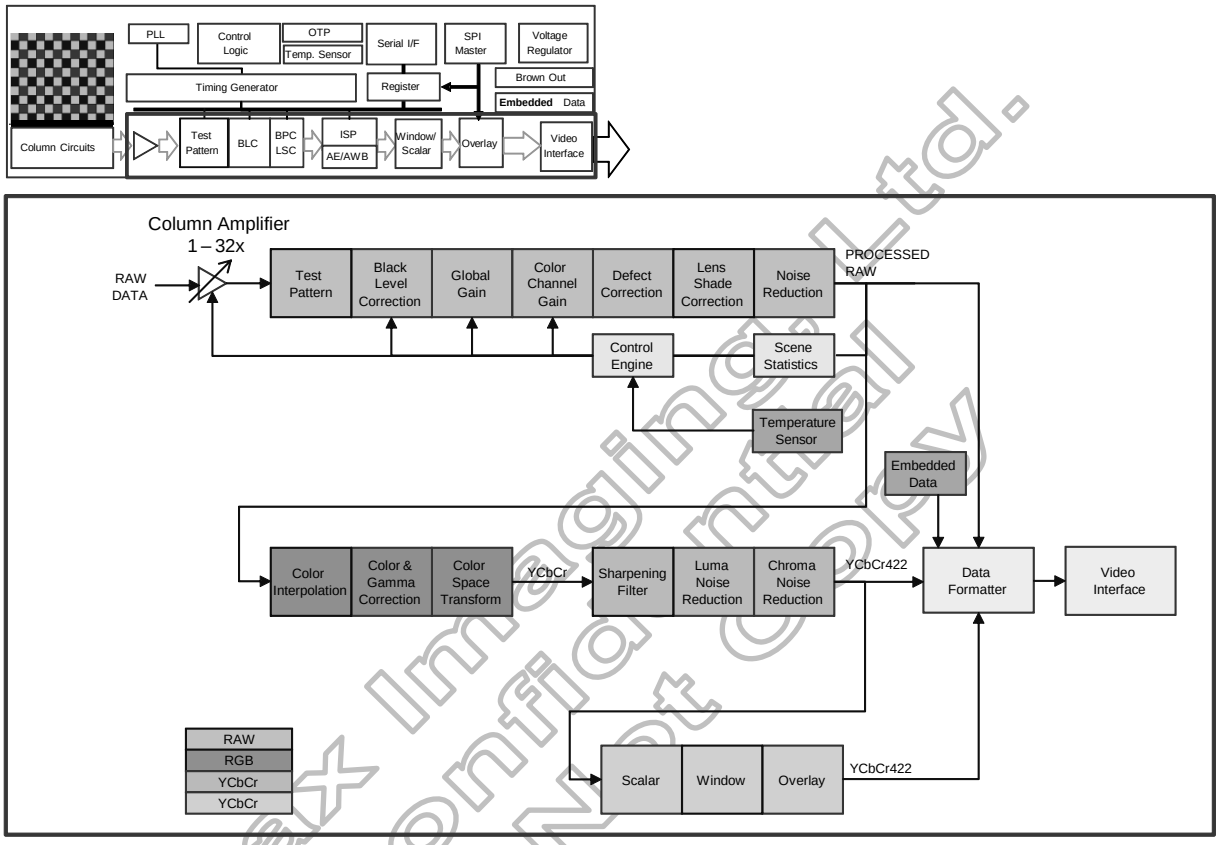


Figure 4.1: ISP signal chain

4.1. Test pattern

HM1246-AWD offers 16 different RAW data test patterns detailed in the table below.

Test pattern	Register value 0x0601[7:4]	Description
B & W square	0000	Pixel value alternates between 255 and 0 every 8th row and 8th column.
Gray blending	0001	Pixel value increases by 6DN every 8th column from 0 – 966DN.
Walking 1's	0010	Pixel values increases by 1LSB every column from 0 – 1023DN.
Color Bar Blending	0011	6 color bars where pixel values increases by 4DN every 4th row from 0 – 972DN.
Color Bar	0100	6 color bar with fixed pixel values; color changes every 216th column.
R Color Blending 6	0101	Red color where pixel value increases by 6DN every 8th column from 0 – 966DN.
R Color Blending 25	0110	Red color where pixel value increases by 25DN every 32nd column from 0 – 1000DN.
R Color Blending 50	0111	Red color where pixel value increases by 50DN every 64th column from 0 – 1000DN.
G Color Blending 6	1000	Green color where pixel value increases by 6DN every 8th column from 0 – 966DN.
G Color Blending 25	1001	Green color where pixel value increases by 25DN every 32nd column from 0 – 1000DN.
G Color Blending 50	1010	Green color where pixel value increases by 50DN every 64th column from 0 – 1000DN.
B Color Blending 6	1011	Blue color where pixel value increases by 6DN every 8th column from 0 – 966DN.
B Color Blending 25	1100	Blue color where pixel value increases by 25DN every 32nd column from 0 – 1000DN.
B Color Blending 50	1101	Blue color where pixel value increases by 50DN every 64th column from 0 – 1000DN.
Value 512	1110	All pixel values are 512.
Solid Color	1111	Set different values in different channels by setting registers 0x0602 ~ 0x0609.

Table 4.1: Test pattern

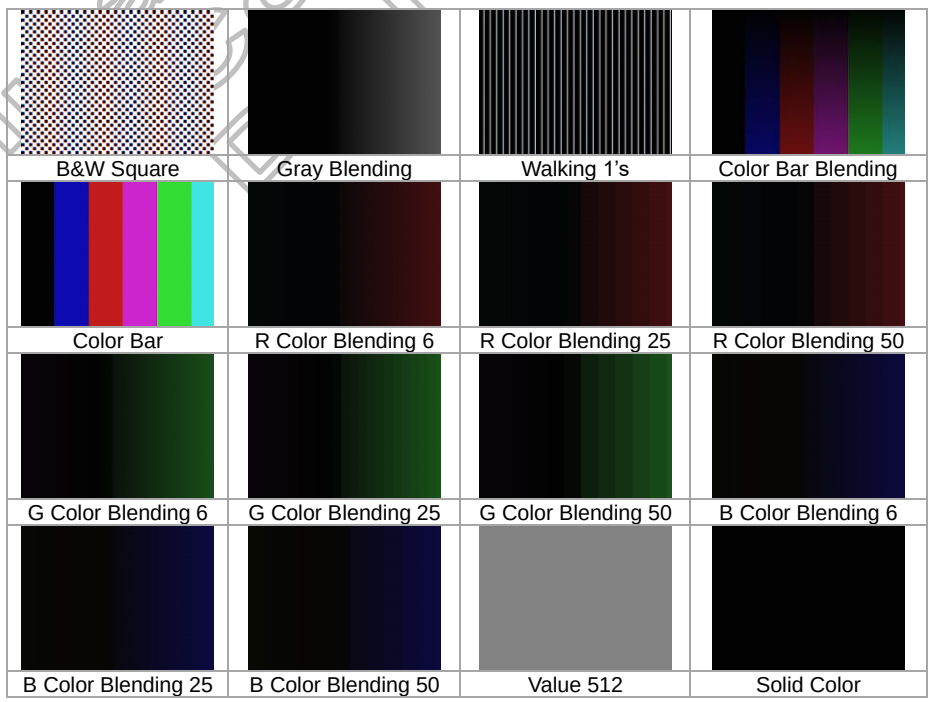


Figure 4.2: Test image patterns

4.2. ISP functions

RAW ISP block	Description
Black Level Calibration	Track shielded pixel value to adjust the black level of each frame to the programmed target mean value.
Digital Gain	Global digital gain are programmed in 2.6 fixed point number **(2 integer bits, 6 fractional bits)**, and channel gain are programmed in 3.6 fixed point number **(3 integer bits, 6 fractional bits)**.
Defect Pixel Correction	Identifies and corrects hot and cold pixel defects by comparing each pixel to neighboring same-color pixels.
Lens Shade Correction	The lens and module assembly can reduce the illumination and induce visible hue shift at the peripheries of the sensor array. To minimize this effect, the Lens Shading Correction circuit compensates this effect by applying a grid-based correction factor to the pixel data as a function of distance from the programmed lens center. To avoid applying correction in areas outside of the image circle, the LSC can be programmed to compensate only the region within the specified radial distance from the window center as shown in Figure 4.4.
Bayer Pattern Interpolation	Bayer to RGB conversion.
Color Correction Matrix	Programmable 3x3 matrix to map the color response of the sensor to a desired target. The matrix values are determined based on the spectral response and the cross talk characteristics of the sensor. A mode is provided to interpolate the effective correction matrix between two programmed matrices based on the spectral response of the sensor to different light color temperatures.
Gamma Correction	The gamma curve is comprised of a piece-wise linear curve, which is applied equally to the R, G and B color channel. The input data points are as follows: 4, 8, 16, 32, 40, 48, 56, 64, 72, 80, 96, 112, 144, 176, 208 and 255.
Luma and Chroma Denoise	Noise reduction is applied separately to the luminance **(Y)** channel and chrominance **(CbCr)** channel. The luminance noise reduction algorithm is edge-sensitive with configurable thresholds to balance the integrity of the edge with noise reduction.
Sharpening	2-dimensional sharpening filter can be applied to the luminance component of the image.
Contrast Adjustment	Contrast adjustment consists of a 7 segment piecewise linear curve which provides flexibility to program different contrast schemes from the basic linear contrast to segment s-curve contrast.
Brightness Adjustment	Brightness adjustment adds or subtracts an offset of the luminance channel.
Color Adjustment	Color adjustment controls the saturation and hue in the UV domain.

Table 4.2: ISP functions

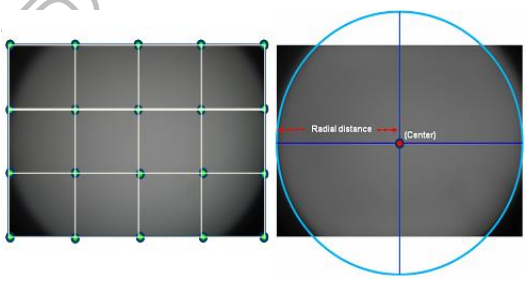


Figure 4.3: Lens shade compensation with corner limit

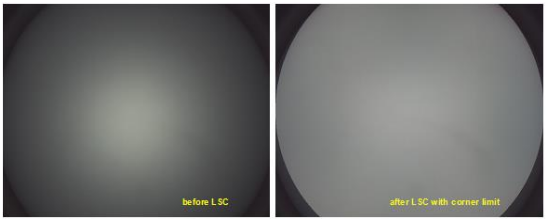


Figure 4.4: Sample image before and after lens shade compensation

4.3. Automatic Exposure Gain (AEG)

The Automatic Exposure Gain **(AEG)** analyzes the luminance statistics and conditionally adjusts the exposure and gain of the sensor to the user-defined target value. Programmable registers can set modes, targets, limits, filters and hysteresis settings.

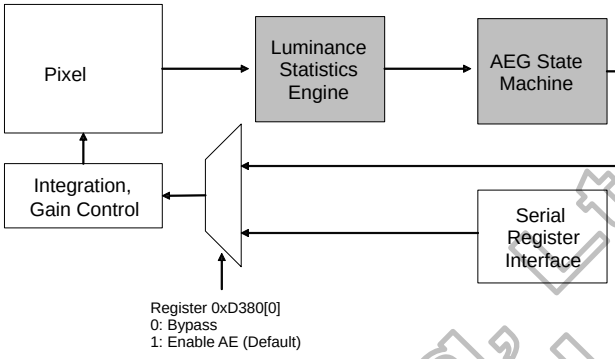


Figure 4.5: Auto exposure gain block diagram

4.3.1. Luminance statistics engine

The frame Brightness Value **(BV)** is a computed weighted average of luminance level from 25 windows and 1 Region of Interest **(ROI)**. The starting coordinate of the first window, the size of the window, and the individual weighting of each window are programmable. The starting and ending coordinate of the ROI and the weight are programmable. The computed brightness value can be read from the register AE_AVG_BV **(0xD3C2)**, and from the Embedded Line **(see Embedded Line section)**.

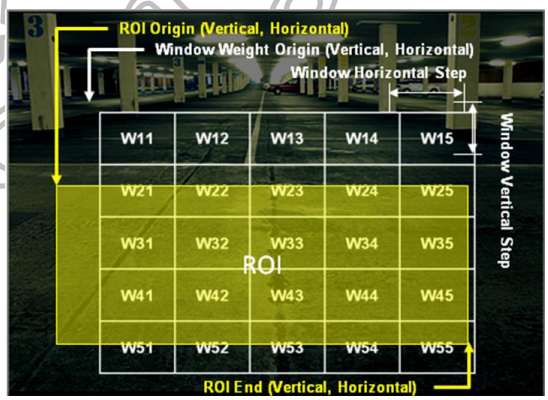


Figure 4.6: AE statistics

4.3.2. AEG state machine

The AEG State Machine adjusts the integration, analog gain and digital gain against the target brightness value. Three convergence zones with programmable damping factors balance speed and stability. In the Fast Zone, larger exposure gain steps are applied to quickly converge to the target brightness value. In the Slow Zone, smaller exposure gain steps are applied to smoothly converge to the target brightness value. Inside the target zone, the control loop does not change exposure gain values.

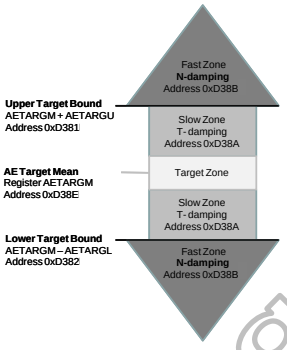


Figure 4.7: AE zones

Address	Register name	Description
0xD38F	AEMXEXH	AE maximum exposure setting high byte **(MSB)**
0xD390	AEMXEXL	AE maximum exposure setting low byte **(LSB)**
0xD391	AEMNEX	AE minimum exposure setting
0xD392	AEMXAG	AE setting of maximum coarse analog gain
0xD393	AEMXDG	AE setting of maximum digital gain and fine analog gain
0xD394	AEMNDG	AE setting of minimum digital gain

Table 4.3: AEG max and min limits

4.3.3. Flicker intervals

Exposure intervals of 1/100 and 1/120 second are using to avoid 50Hz and 60Hz flicker from artificial light, respectively. The exposure interval should follow the equations below:

Total Integration Time = INTG (register programmable number of rows) × t_{LINE}
INTG (60Hz Flicker Step) = (1/120) / t_{LINE}
INTG (50Hz Flicker Step) = (1/100) / t_{LINE}

When the AEG control loop is enabled, the exposure interval can be programmed and selected between 50Hz and 60Hz. If flicker step is not required, simply set the interval to 1.

Address	Flicker function	Description
0xD120[0]	Flicker Selection	0 = 50Hz, 1 = 60Hz
0xD542[7:0] **(high byte)** 0xD543[7:0] **(low byte)**	50Hz INTG interval	Flicker interval for 50Hz
0xD540[7:0] **(high byte)** 0xD541[7:0] **(low byte)**	60Hz INTG interval	Flicker interval for 60Hz
0xD54F[7:0]	Flicker Hysteresis	Hysteresis value to delay sub-flicker step integration time for AEG

Table 4.4: Automatic exposure gain flicker control registers

4.4. Automatic White Balance (AWB)

Automatic White Balance **(AWB)** block adjusts the color gain of the sensor under different color temperatures based on the white pixel region of the scene based on color temperature estimation. The AWB can be bypassed through the serial register.

4.5. Overlay engine

The HM1246-AWD features two embedded overlay engines with independent color, location, transparency, blink and timeout function. When the overlay engines are enabled, the content of the overlay image is transferred from the external memory to the embedded memory through the SPI interface. Up to 1 Megabyte of compressed overlay images can be stored in the external memory.

The overlay engines decompress the overlay data in the buffer and blend the graphic images with the streaming video data. The maximum overlay data image size can be 640 x 480, which can be rendered up to 1280 x 960 pixels by using H / V 2x scale mode. Each overlay image has independent palette of up to 8 colors out of 8192 colors and up to 8 transparent levels.

Two overlay layers may be blended simultaneously with individually programmable line height, width, and coordinate. The first overlay engine can be used to display a static graphic image. The second layer can be used to display a second set of static graphic images or a dynamic overlay layer. For dynamic overlay, a new image file can be transferred from the SPI memory to the allocated internal buffer during streaming. Host can enable and disable overlay function by controlling “OVEN”. If “OVEN” is low, the overlay engines will be disabled. The block diagram of the Overlay Engines is shown in the figure below.

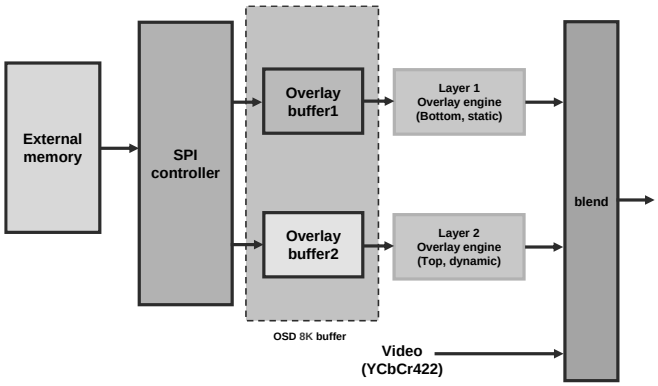


Figure 4.8: Block diagram of overlay engines

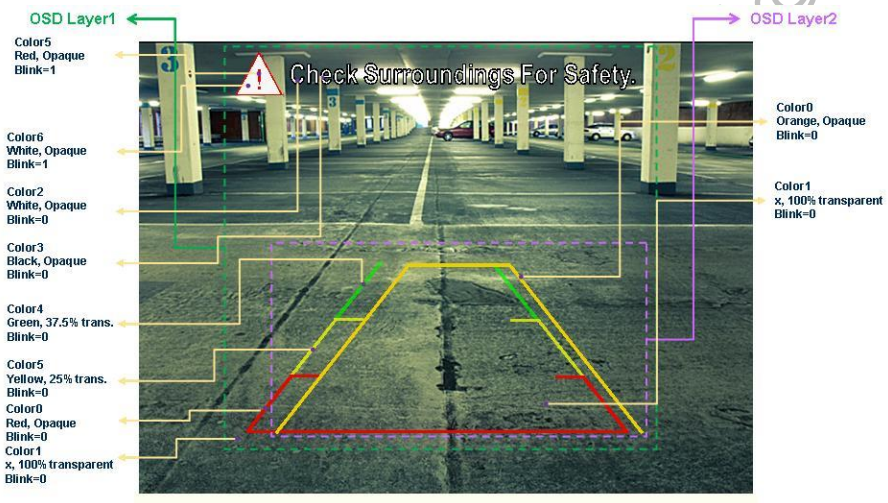


Figure 4.9: Static overlay engine example

4.5.1. Blink and timeout function

Both overlay engines support independent blink and timeout function. If the blink function is enabled, the overlay engine flash the graphic image on and off repeatedly. If the timeout function is enabled, the overlay engine will display the graphic image for a specified period.

4.6. Digital window

Digital window adjusts the frame output to an arbitrary size and location without change to the frame timing. The window size is programmed by specifying x **(horizontal)** and y **(vertical)** starting and size. For color sensor, the DWIN_XOFFSET / DWIN_YOFFSET should be set to an even pixel coordinate to maintain the color order.

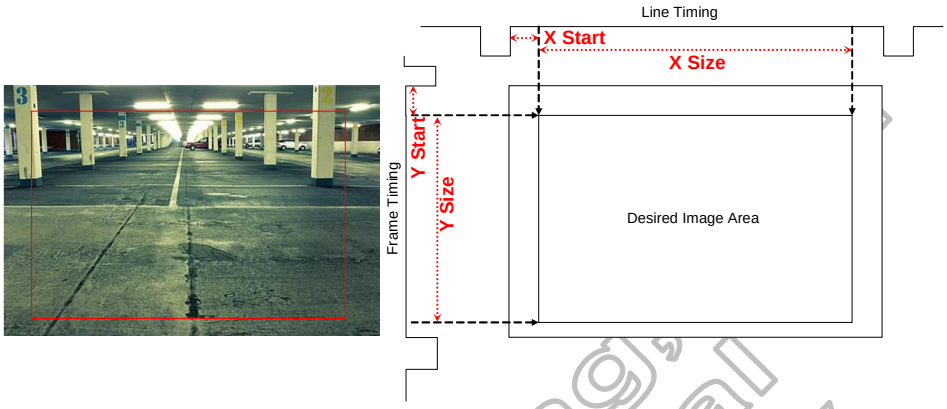


Figure 4.10: Windowing

Address	Register name	Value
0xD5E4	DWIN_XOFFSET_H	0x00
0xD5E5	DWIN_XOFFSET_L	0x08
0xD5E6	DWIN_XSIZE_H	0x05
0xD5E7	DWIN_XSIZE_L	0x00
0xD5E8	DWIN_YOFFSET_H	0x00
0xD5E9	DWIN_YOFFSET_L	0x08
0xD5EA	DWIN_YSIZE_H	0x03
0xD5EB	DWIN_YSIZE_L	0xC0

Table 4.5: Default settings of digital window

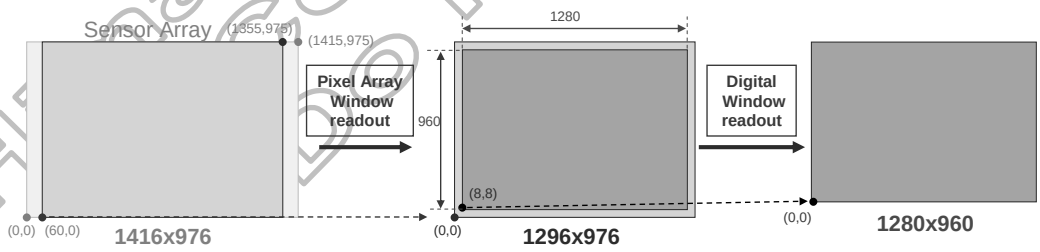


Figure 4.11: Spatial illustration of default digital window readout

4.7. Scaling

4.7.1. Up-Scaling

HM1246-AWD supports video upscaling function with scale factor range from 1x to 2x. For full resolution application, the scalar can convert the video signal from 640 x 480 ~1280 x 960 to an output of 1280 x 960.

Below is an example that upscaling function is used to convert from 1024x768 to 1280x960 with the scale factor=1.25X **(Using 0.8X area of the original video)**. The optical center after upscaling is the same as the pixel array optical center.

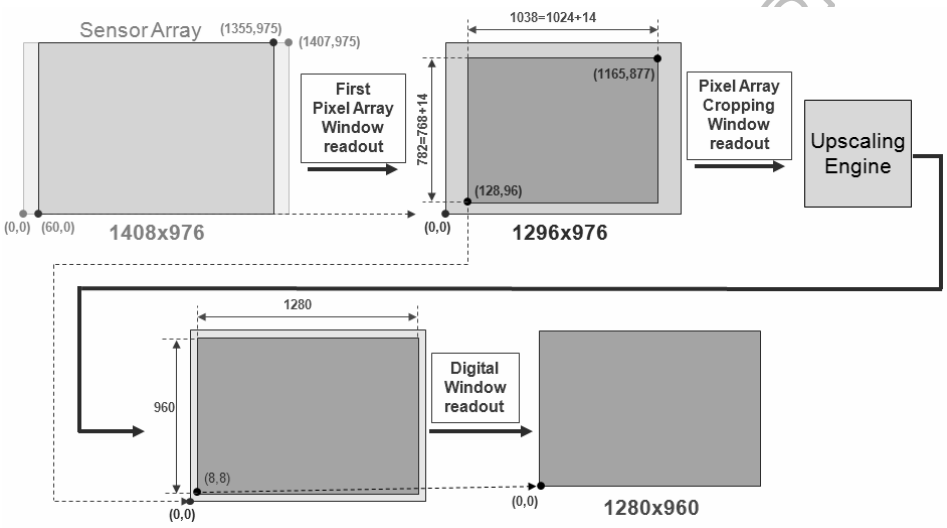


Figure 4.12: Spatial illustration of upscaling engine with scale factor=1.25X

First pixel array window readout			Pixel array cropping window readout		
Address	**Register name**	**Value**	**Address**	**Register name**	**Value**
0x351	X_LA_START_H	0x00	0x0344	X_ADDR_START_H	0x00
0x352	X_LA_START_L	0x3C	0x0345	X_ADDR_START_L	0x80
0x353	X_LA_END_H	0x05	0x0346	Y_ADDR_START_H	0x00
0x354	X_LA_END_L	0x4B	0x0347	Y_ADDR_START_L	0x60
0x355	Y_LA_START_H	0x00	0x0348	X_ADDR_END_H	0x04
0x356	Y_LA_START_L	0x00	0x0349	X_ADDR_END_L	0x8D
0x357	Y_LA_END_H	0x03	0x034A	Y_ADDR_END_H	0x03
0x358	Y_LA_END_L	0xCF	0x034B	Y_ADDR_END_L	0x6D

Digital window readout			Scale factor		
Address	**Register name**	**Value**	**Address**	**Register name**	**Value**
0xD5E4	DWIN_XOFFSET_H	0x00	0xD5F0	SCAL_HSF_H	0x03
0xD5E5	DWIN_XOFFSET_L	0x08	0xD5F1	SCAL_HSF_L	0x33
0xD5E6	DWIN_XSIZE_H	0x05	0xD5F2	SCAL_VSF_H	0x03
0xD5E7	DWIN_XSIZE_L	0x00	0xD5F3	SCAL_VSF_L	0x33
0xD5E8	DWIN_YOFFSET_H	0x00			
0xD5E9	DWIN_YOFFSET_L	0x08			
0xD5EA	DWIN_YSIZE_H	0x03			
0xD5EB	DWIN_YSIZE_L	0xC0			

Table 4.6: Example of upscaling engine with scale factor=1.25x

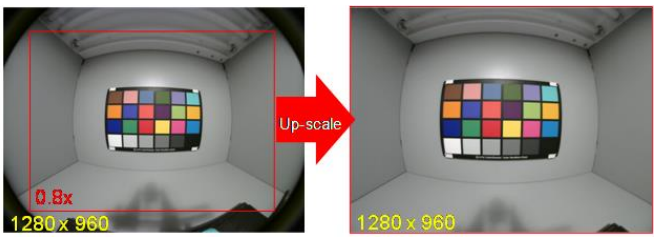


Figure 4.13: Video upscaling example

4.7.2. Down-Scaling

HM1246-AWD supports video down-scaling function with the specified resolutions listed in application note. For more details, please consult with Himax Imaging.

4.8. Synchronization function

4.8.1. FSIN function

HM1246-AWD supports frame synchronization to an external sync signal. When enabling FSIN **(Frame Sync Input)** function **(set register 0x5290=0x02)**, the HM1246-AWD will be placed into slave mode and wait for the host to issue trigger signal **(FSIN)** to do initiate the operation. The first FSIN will trigger video timing and use subsequent FSIN pulse for frame alignment.

4.9. LED control & IR-cut switch function

HM1246-AWD provide simple controller for LED and IR-cut switch control. When using CDS photo resistor to sense light intensity the controller can output control signal to control external LED on/off and to switch IR-cut filter. The control method is depicted in the following figure.

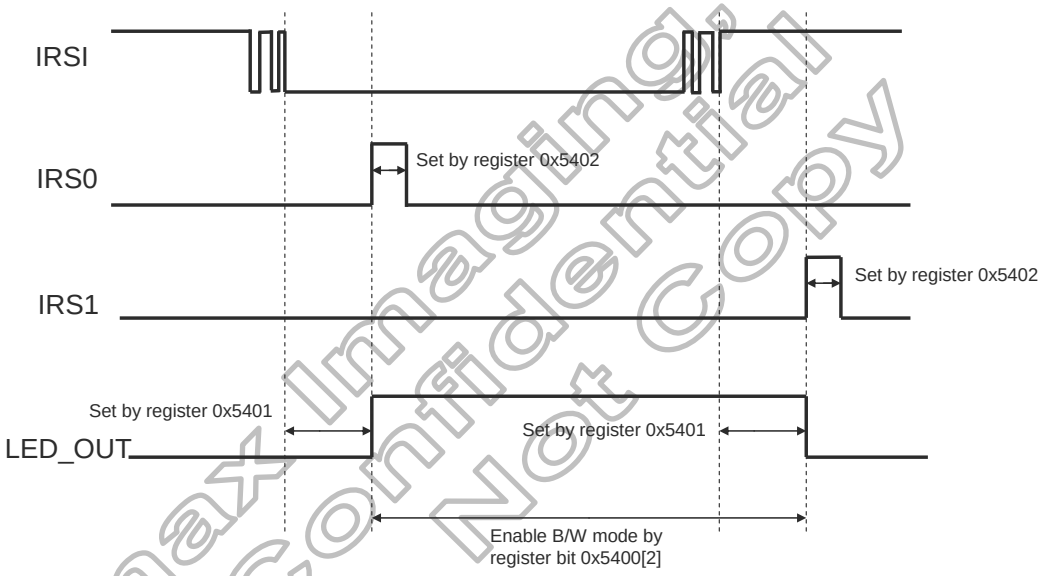
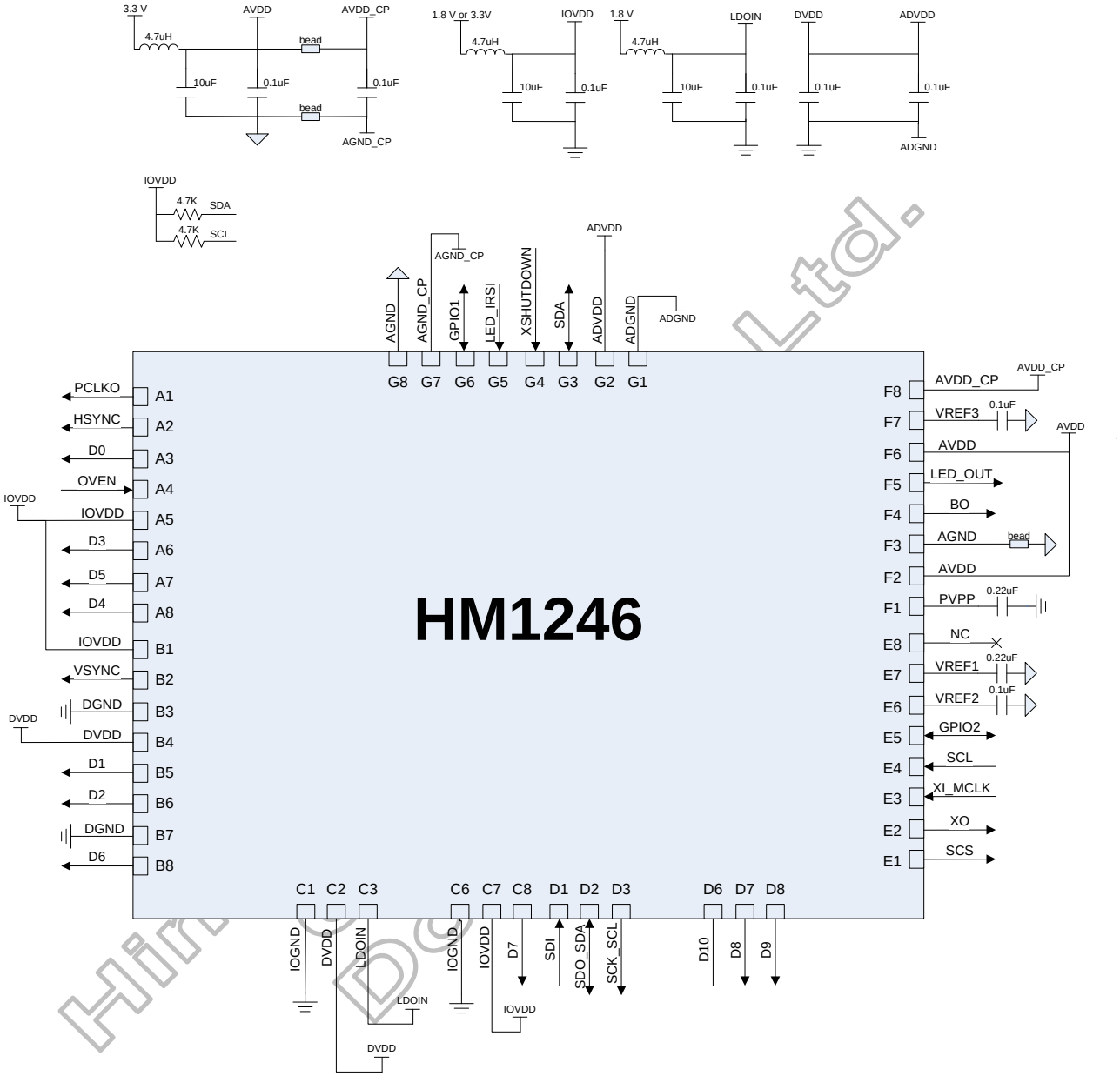


Figure 4.14: LED and IR-cut control

5. Typical Application Circuit

5.1. Internal LDO mode (CSP)



Note: (1) 8-bit data format should use D0 ~ D7. 10-bit data format should use D0 ~ D9.
(2) CCI pull-up resistors should have a value based on the CCI specification **(typically 4k7 ohm)**.
(3) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
(4) When using internal OTP charge pump to generate 7.5V for write operation, the PVPP pin should not be connected to any external supply-voltage or ground
(5) When using external PVPP mode, supply 7.5V to PVPP pin. The pin should be left floating if OTP is not being programmed.
(6) AGND and DGND should be separated and connected to a single point outside the module.

Figure 5.1: Application circuit for CSP using internal LDO

5.2. Reference clock

Reference clock can be provided by an external oscillator from 6 – 27MHz. In this case, the clock is connected to the XI_MCLK pin, and the XO pin is left unconnected. The sensor can also be connected to a crystal oscillator using the circuit shown in the figure below. Please contact Himax Imaging for the recommended component values.

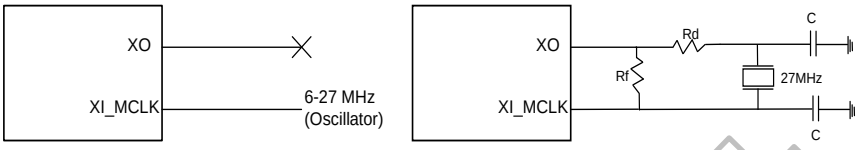


Figure 5.2: Reference clock using external oscillator (Left) and crystal oscillator (Right)

5.3. Boot strap sensor configuration pins

The HM1246-AWD offers 11 bootstrap pins shared with the parallel data output ports **(D0 ~ D9)**, HSYNC and VSYNC ports. These shared ports are bootstrap input pins with their values sampled 200μs after XSHUTDOWN transitions to a high state **(please see Power Up Sequence diagram)**. After sampling, these shared ports become tri-stated or driven low based on the port configuration. The user need to add external pull-up /pull-down resistors on these shared ports to assign the settings of the bootstrap pins. For more detailed information, please refer to 6.7 System boot controller.

6. System Level Description

6.1. Operating modes

The HM1246-AWD supports modes of operation as shown in Table 6.1: HM1246-AWD operating modes.

Mode	Description	Power	Register values	Circuit status						
				IO	VDD_BO	I2C	OSC	PLL	Digital	TEMP sensor
Power Off	No power supplied to sensor	OFF	NA	High-Z	-	-	-	-	-	-
Shutdown	Very low power hardware shutdown	ON	Default	High-Z	OFF	OFF	OFF	OFF	OFF	OFF
Stop_Self	Circuits active, no video	ON	Reset → Default Others → Retained	High-Z or Low	ON	ON	ON	ON	Standby Mode	ON
Stop_Auto	Circuits active, Boot Strap pin sampled, automatic loading initialization if boot strap pin BOOT = 1, no video	ON	Default or overwritten by boot commands	High-Z or Low(1)	ON	ON	ON	ON	Standby Mode	ON
S/W Standby	Low-power consumption, no video	ON	Retained	High-Z or Low(1)	ON	ON	ON	OFF	Standby Mode	OFF
Streaming	Streaming video on the parallel output port	ON	Retained	Active	ON	ON	ON	ON	ON	ON

Note: (1) Programmable IO to High Impedance or drive low

Table 6.1: HM1246-AWD operating modes

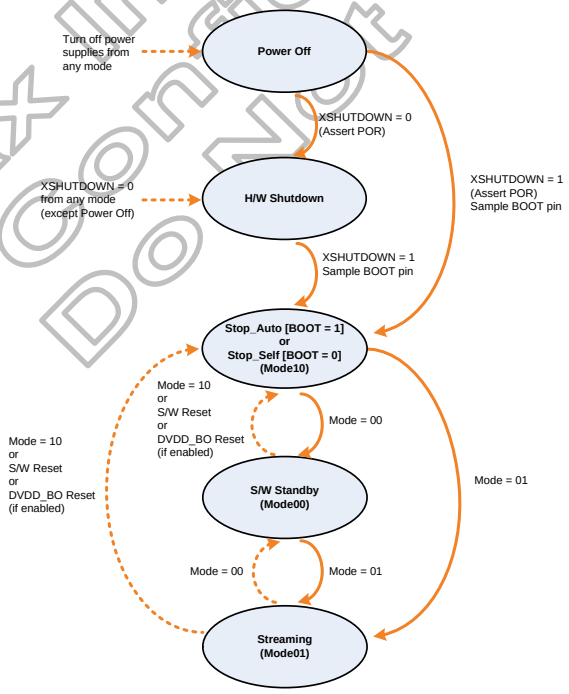


Figure 6.1: State diagram

6.2. Reset

The HM1246-AWD provides four reset methods: Power On Reset **(POR)**, Hardware Reset **(XSHUTDOWN)**, Brown Out Reset **(BOR)** and software reset.

6.2.1. Power On Reset (POR)

An internal POR circuit applies a system reset until the DVDD supply reaches a monitored voltage threshold. This insures that the supply voltage is stable and the sensor is properly initialized.

6.2.2. Hardware reset

After all the power rails are settled, hardware reset is triggered by toggling XSHUTDOWN pin.

6.2.3. Software reset

Software reset is applied by writing register value 1 to register bit SW_RESET[0] (0x0103[0]). When reset is applied, the sensor will return to “Stop mode” and reset all serial interface registers to its default values.

6.2.4. Brown Out Reset (BOR)

The BOR circuit continuously monitors the digital supply voltage and asserts a system reset when the supply voltage falls below the programmed supply threshold **(1.0V, 1.1V, 1.2V, 1.3V)**. The circuit is designed to respond to low bandwidth events, as such would filter glitch events of approximately 1µs or less.

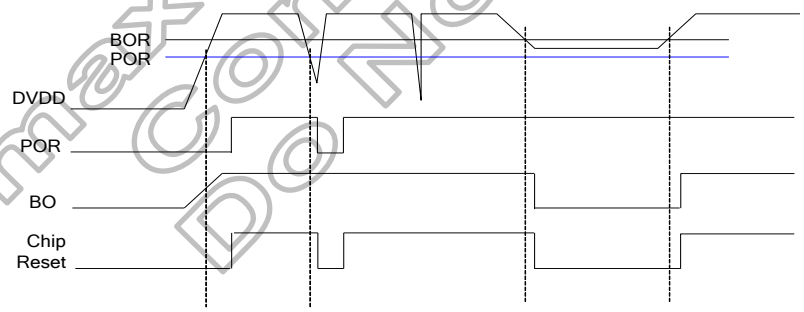


Figure 6.2: POR and BOR reset

6.3. Power up sequence

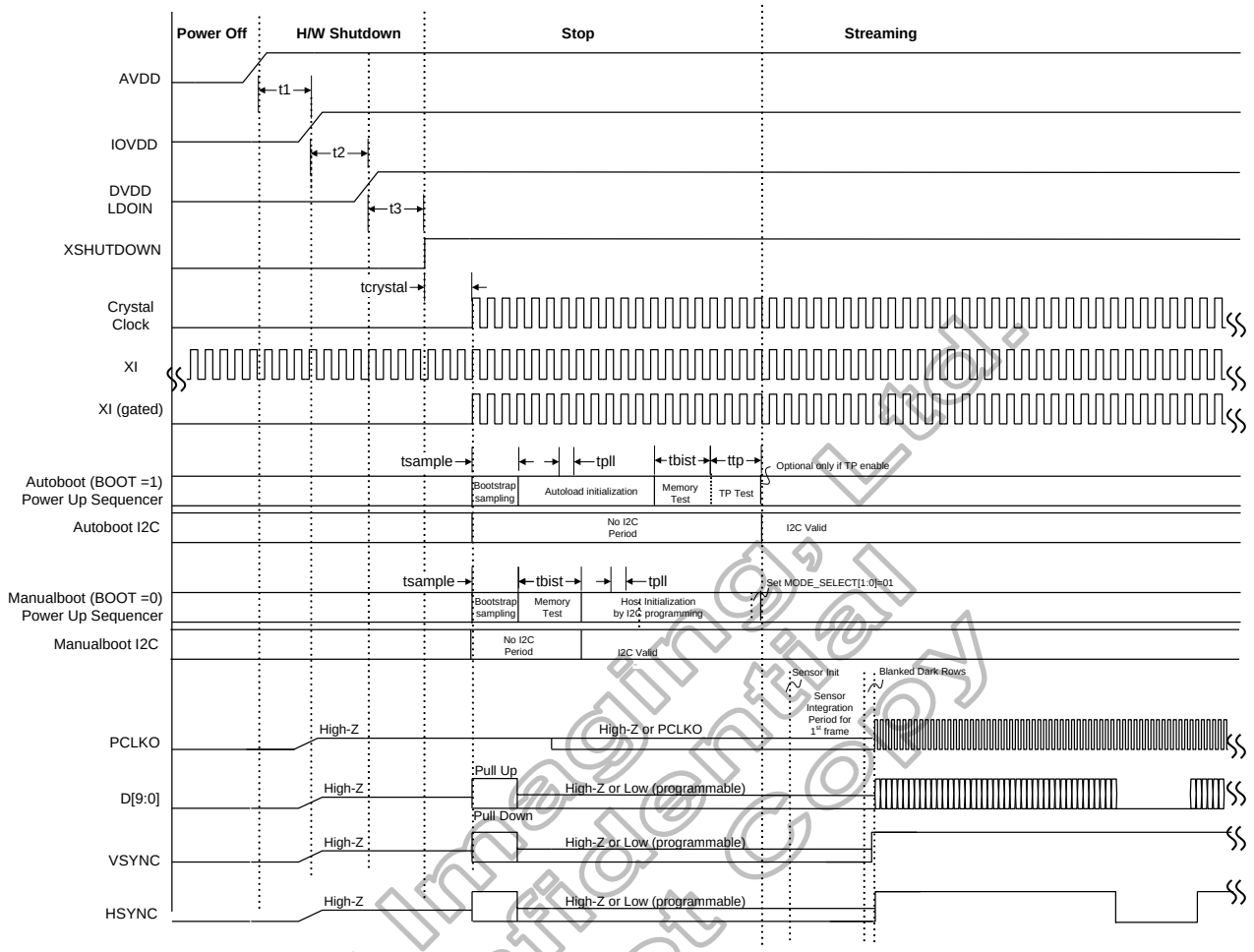


Figure 6.3: Power-up sequence

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
AVDD to IOVDD	t1	0	-	∞	s
IOVDD to DVDD/LDOIN	t2	0	-	∞	s
DVDD/LDOIN to XSHUTDOWN	t3	0	-	∞	s
XSHUTDOWN to crystal clock oscillation **(if using crystal)**(1)	$t_{crystal}$	-	650	-	µs
Sample bootstrap pin	t_{sample}	200	-	2000	µs
PLL lock time	t_{pll}	-	100	-	µs
Built in self test	t_{bist}	-	-	3000	µs
Optional test pattern chip test	t_{tp}	-	41.8	-	ms

Note: (1) The period is dependent on the external crystal circuit.

Table 6.2: Power-up sequence timing

6.4. Power down sequence

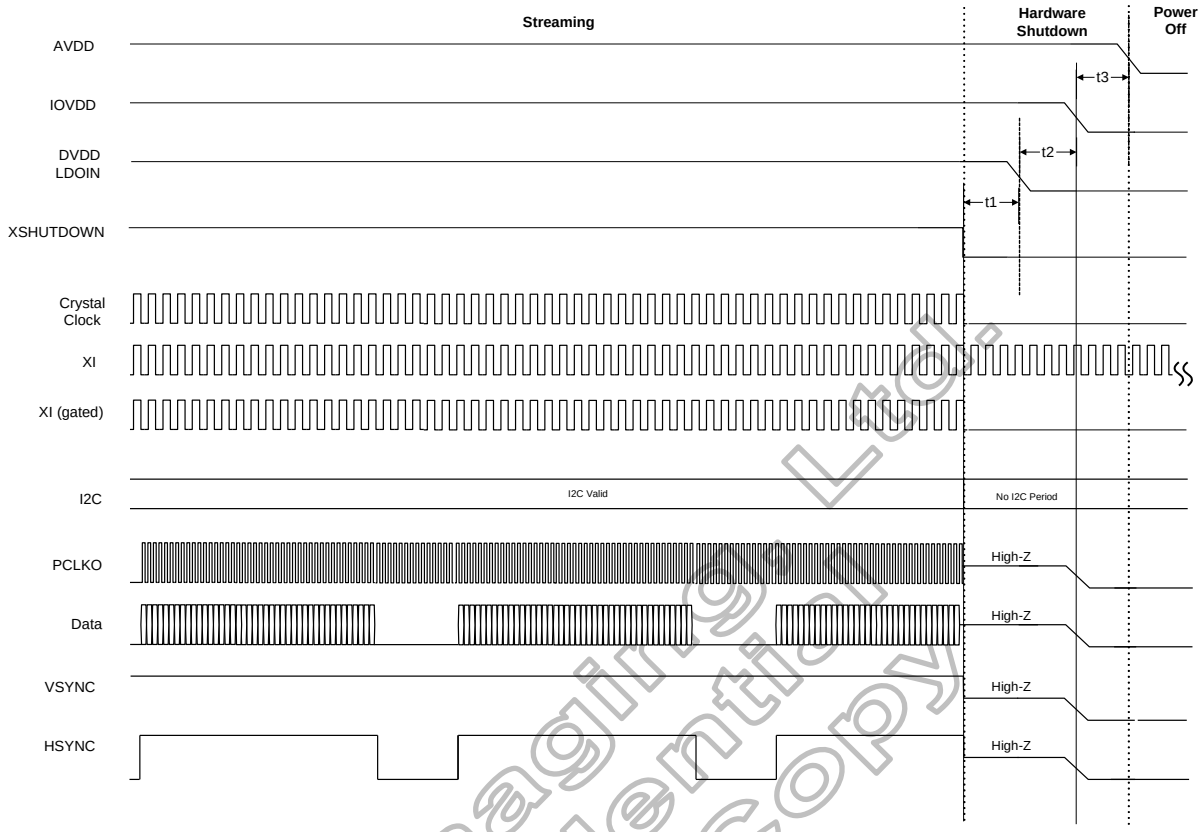


Figure 6.4: Power-down sequence

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
XSHUTDOWN to DVDD/LDOIN	t1	0	-	∞	s
DVDD/LDOIN to IOVDD	t2	0	-	∞	s
IOVDD to AVDD	t3	0	-	∞	s

Table 6.3: Power-down sequence timing

6.5. Clock generation

The sensor system clock can be generated by the on-chip Phase Lock Loop or can be bypassed to use the external clock source.

- The PLL is disabled during Hardware Shutdown mode and after software reset.
- The PLL can be enabled by setting register bit PLL_EN **(0x2003[0])** to 1. The register's default value is 0
- The clock source can be switched to PLL by first programming the PLL registers and then writing register bit CKCFG **(0x2F01[7])** to 0.
- PLL Input Range = 1 ~ 2.5MHz
- VCO_OUT = MCLK / (0x0305[5:1] + 1) * (2 + 0x0305[0]) * (0x0303[7:0] + 1) with range from 360~680MHz
- SYS_CLK = VCO_OUT / (0x0307[5:4] * 0x0307[7:6])
- PCLKO_CLK **(vt_pix_clk)** = VCO_OUT / (0x0307[2:0] * 0x0307[7:6])

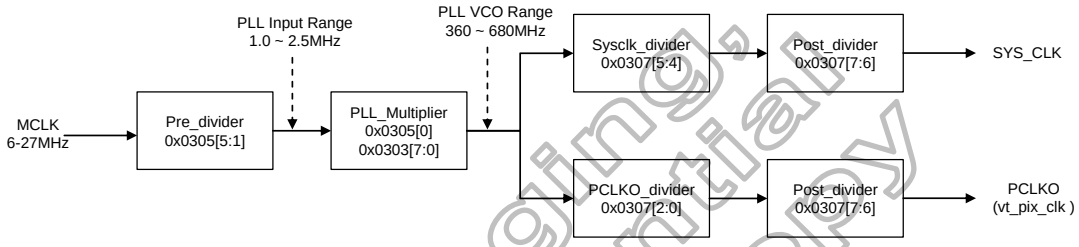


Figure 6.5: Clock generator

6.6. Memory interface and configuration

6.6.1. I2C EEPROM

The HM1246-AWD supports I2C master to interface with an external I2C EEPROM. When the mode of operation is in **Streaming** or **Stop**, the user can access the external I2C EEPROM through the I2C slave port. The user simply issues I2C commands targeting the I2C EEPROM with its I2C ID and HM1246-AWD will pass along the I2C transferred data back and forth. The figure below shows the diagram of I2C EEPROM access operation.

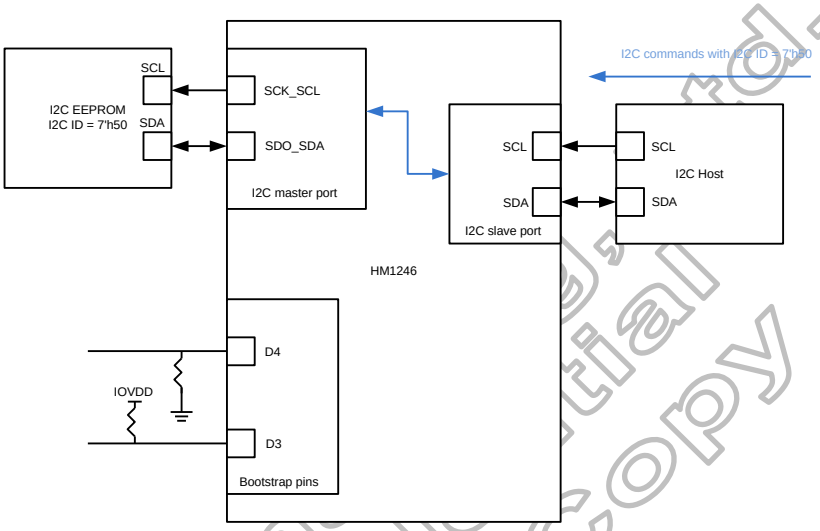


Figure 6.6: I2C EEPROM access operation diagram

6.6.2. SPI memory access

HM1246-AWD supports a standard SPI Master port which supports read and write commands, which can be used to interface with an external memory to load overlay content and register settings. When the mode of operation is in **Streaming** or **Stop**, and the overlay display function is disabled, the user can access the external SPI device through the I2C slave port by issuing I2C commands targeting the SPI programming interface to initiate the SPI access.

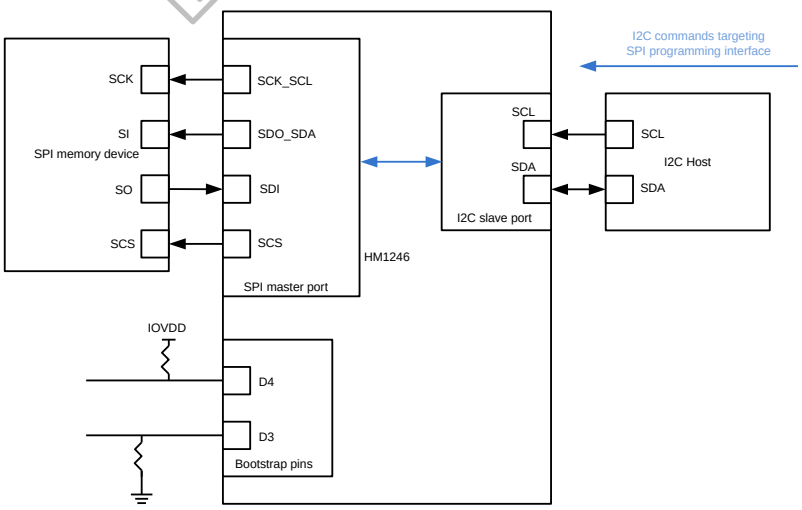


Figure 6.7: SPI memory access operation diagram

HM1246-AWD supports in-system programming of SPI EEPROM / FLASH by tri-stating the SPI ports during Hardware power down **(XSHUTDOWN=0)** or by setting the interface configuration registers.

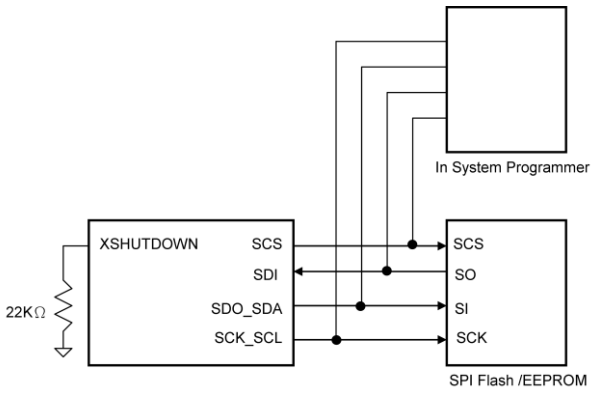


Figure 6.8: SPI bus with in system programmer

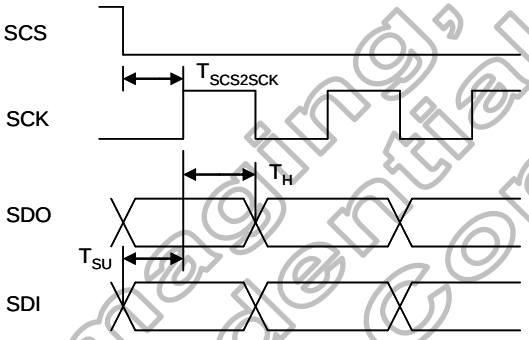


Figure 6.9: SPI timing diagram

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
SPI SCK frequency	f_{SPI_CLOCK}	-	21.25	42.5	MHz
SCS setup time	$T_{SCS2SCK}$	-	23	-	ns
Setup time	T_{SU}	-	-	22	ns
Hold time	T_H	-	-	22	ns

Table 6.4: SPI output timing

6.7. System boot controller

The HM1246-AWD features a System Boot-up Controller **(SBC)** block that is responsible for the boot-up operation. The sensor supports three boot options to initialize the sensor:

- Manual mode relies on external initialization by the host through I2C interface
- Automatic boot by the sensor from the on-chip OTP
- Automatic boot by the sensor from the on-chip OTP followed by external SPI Flash or EEPROM.

The boot up sequence is selected by the setting of the bootstrap pins which are listed in Table 6.5: Configuring auto-boot options**,** and requires valid content in the internal OTP and the external I2C/SPI memory device.

6.7.1. Chip configuration

HM1246-AWD provides a flexible method to configure chip functions. The auto-boot options can be configured by the states of bootstrap pins. The detailed information is listed in Table 6.5: Configuring auto-boot options.

Boot function	Pin name	Internal PU/PD	State	Selection	State register
BOOT	D8	PU	L	Boot by an external controller	BOOT **(0x2000[6])**
			H	**Self-booted**	
External Memory configuration	{D4,D3}	{PD,PD}	**{L,L}**	**no external memory**	MEM_CFG[1:0] **(0x2001[3:2])**
			{L,H}	I2C EEPROM	
			{H,L}	SPI EEPROM / FLASH	
External Memory Size	D5	PD	**L**	**I2C EEPROM: support 11-bit address (3-bit in control byte & 8-bit in address byte)** **SPI EEPROM / FLASH: support 2-byte address**	MEM_SIZE **(0x2000[7])**
			H	I2C EEPROM: support 2-byte address SPI EEPROM / FLASH: support 3-byte address	

Table 6.5: Configuring auto-boot options

Function	Function is configured by bootstrap pin	Pin name	State	Selection	State register
I2C Device Address	I2C_ID_SEL **(0x2200[0]=0)**	{D1,D0}	**{L,L}**	**I2C device address =0x24 (7-bit)**	I2CID_LSB[1:0] **(0x2001[1:0])**
			{L,H}	I2C device address =0x25 **(7-bit)**	
			{H,L}	I2C device address =0x34 **(7-bit)**	
			{H,H}	I2C device address =0x35 **(7-bit)**	
Black / White mode	BW_SBP **(0x2002[0]=1)**	D9	**L**	**Output color image**	B_AND_W **(0x2000[0])**
			H	Output black & white image	
Vertical Flip	FLIP_SBP **(0x2002[1]=1)**	D7	**L**	**Output normal image**	FLIP **(0x2000[1])**
			H	Output flipped image	
Flicker	FLK_SBP **(0x2002[2]=1)**	{VSYNC,HSYNC}	{L,L}	60Hz	FLICKER[1:0] **(0x2000[3:2])**
			{L,H}	50Hz	
			{H,X}	0xD770[4]=0 By register bit 0xD120[0] 0xD770[4]=1 Auto select by AFD	
Horizontal Mirror	MIRROR_SBP **(0x2002[3]=1)**	D6	**L**	**Output normal image**	MIRROR **(0x2000[4])**
			H	Output mirrored image	

Table 6.6: Configure chip functions by states of bootstrap pins

Function	Function is configured by setting register	Configuration register bit	Value	Selection
I2C Device Address	I2C_ID_SEL **(0x2200[0]=1)**	I2C_ID[6:0] **(0x2201[6:0])**	-	I2C device address = I2C_ID[6:0] **(7-bit)**
Black / White mode	BW_SBP **(0x2002[0]=0)**	B_AND_W **(0x2000[0])**	0	Output color image
			1	Output black & white image
Vertical Flip	FLIP_SBP **(0x2002[1]=0)**	Vertical flip En **(0x0101[1])**	0	Output normal image
			1	Output flipped image
Flicker	BOOT=H & FLK_SBP **(0x2002[2]=0)**	FLICKER[1:0] **(0x2000[3:2])**	00	60Hz
			01	50Hz
			10/11	0xD770[4]=0 By register bit 0xD120[0] 0xD770[4]=1 Auto select by AFD
	BOOT=L	-	-	0xD770[4]=0 By register bit 0xD120[0] 0xD770[4]=1 Auto select by AFD
Horizontal Mirror	MIRROR_SBP **(0x2002[3]=0)**	Horizontal mirror En **(0x0101[0])**	0	Output normal image
			1	Output mirrored image

Table 6.7: Configure chip functions by registers

6.7.2. Data command format

In automatic boot mode, the formatted boot sequence is stored in the OTP and the external memory device. The boot sequence is stored as a series of write commands with 16-bit address and 8-bit of write data parsed with data tags. The formatted bytes start with “Tag type” byte that has instructions of what the following bytes are used for and the number of commands to be encoded as shown in the following table.

Tag type		Number of address bytes used for updating	Number of data bytes	Automatic bus address increase	Description
[7:4]	[3:0]				
0x1	N	2	N+1	Yes	Continuous (N+1)-byte write
0x2	N	1 **(lower byte)**	N+1	Yes	Continuous (N+1)-byte write
0x4	N	(N+1) x 1 **(lower byte)**	N+1	No	Discrete (N+1)-byte write
0x8	N	0	N+1	Yes	Continuous (N+1)-byte write
0x0	0x0	N/A	N/A	N/A	End of File **(EOF)**

Table 6.8: Tag encoding format

The end of the sequence is indicate by tag 0x00 as End-of-File byte as shown example below.

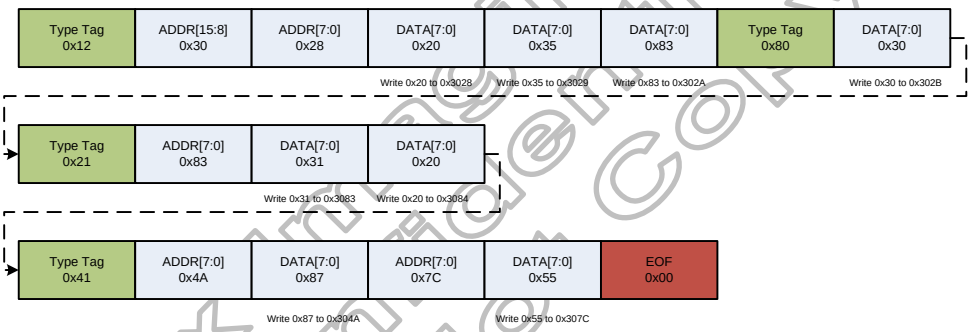


Figure 6.10: Sample initialization with tag and data

6.7.3. Auto-boot from one time programmable memory configuration

The HM1246-AWD provides 3Kb of user programmable memory that can be used to store identification information and sensor initialization registers as part of the auto boot sequence. The OTP is partitioned by 64-byte pages that are accessed through the registers via the I2C interface. The OTP requires 7.5V for programming, which can be supplied externally to the PVPP pad, or supplied internally with a charge pump.

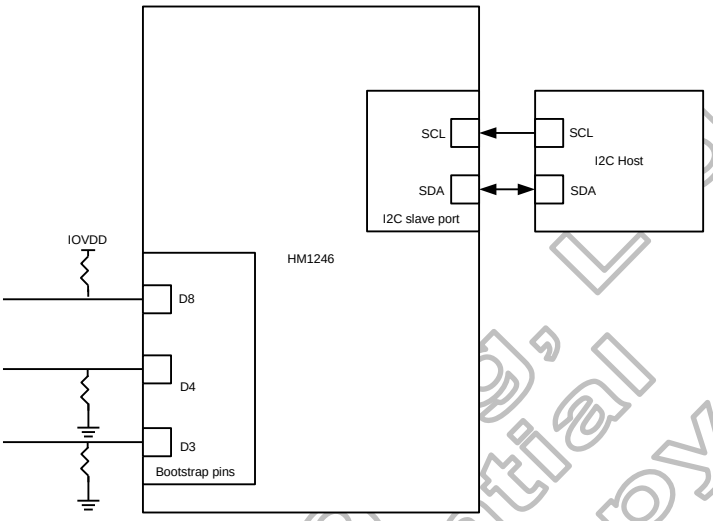


Figure 6.11: Auto-boot from OTP connection setting

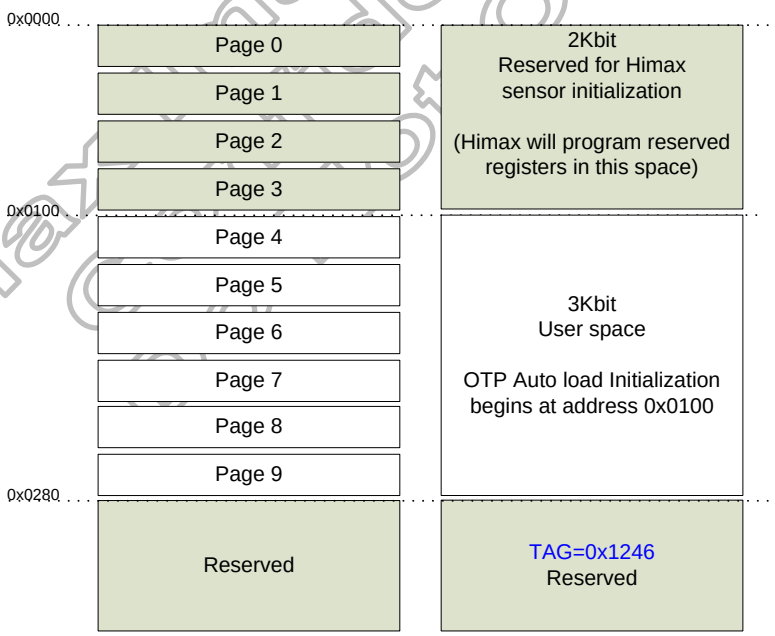


Figure 6.12: On-chip OTP memory partition

6.7.4. Auto-boot from I2C EEPROM configuration

The sensor can boot from OTP and then I2C EEPROM using the connection shown in the figure below. In this mode, the HM1246-AWD will automatically load from the OTP, then I2C EEPROM during the power-up sequence or from one of the reset events.

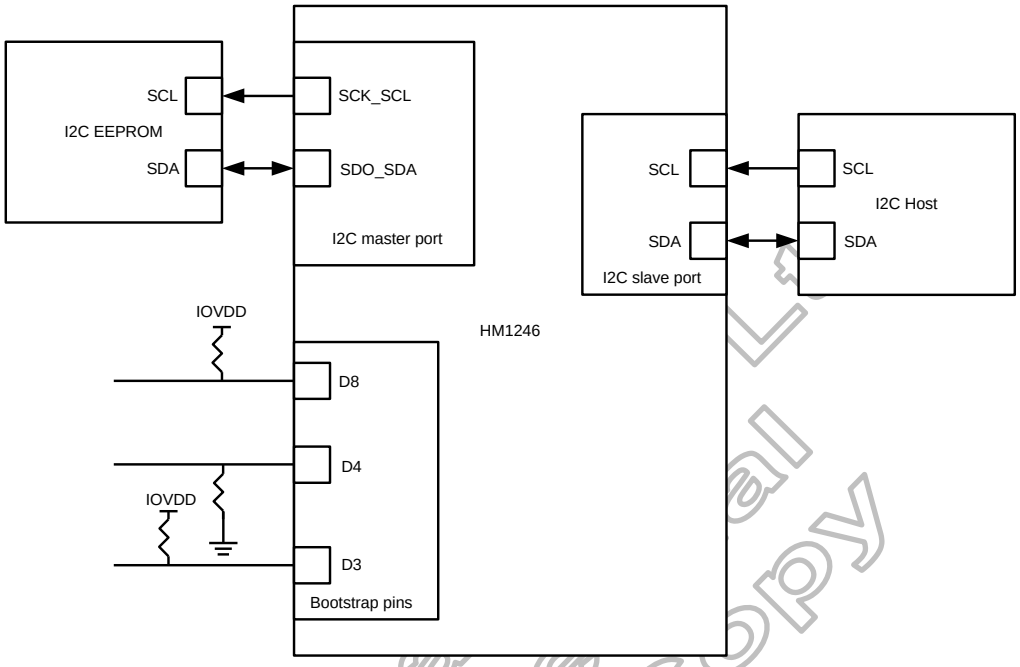


Figure 6.13: Auto-boot from I2C EEPROM mode connection setting

Prior to reading the initialization sequence from the I2C memory, the sensor sends a series of I2C ID bytes to identify the I2C ID of the external device. When the ACK bit of the I2C ID byte is returned 0, the sensor latches the I2C ID value and begins to load instructions from the external device.

The clock frequency of SCL of the I2C master port can be programmed by setting the configuration register I2C_CLK_M **(0x2100)**. The frequency equation is:

$$f_{SCL} = f_{sys} \cdot \frac{1}{2 \cdot (I2C\_CLK\_M + 1)}$$

The variable f_{sys} is the frequency of the system input clock XI_MCLK.

The sensor will load the instructions starting from address 0x00 of the EEPROM, and the load sequence operation is completed once all the instructions are executed. The user configures register bits **MODE_SELECT (0x0100[1:0])** to 0x01 at the end of I2C EEPROM initialization sequence to automatically trigger the mode of operation transition from **Stop (SYS_BOOT_DONE)** to **Streaming**.

6.7.5. Auto-boot from SPI memory configuration

In this setting, HM1246-AWD will automatically load from the OTP, then SPI memory during the power-up sequence or from one of the reset events.

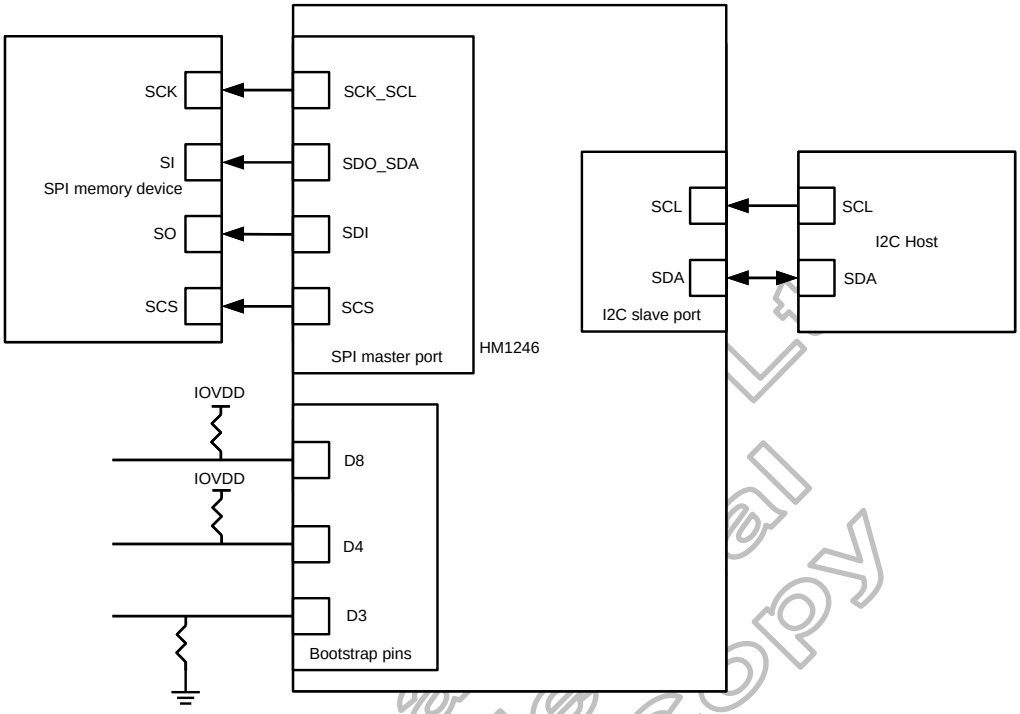


Figure 6.14: Auto-boot from SPI memory mode connection setting

After loading and executing instructions stored in OTP, the sensor loads and execute the Tag Format instructions stored in SPI EEPROM / FLASH memory device starting from the device address 0x00. The load sequence operation is completed once all the instructions are executed. The user configures register bits **MODE_SELECT (0x0100[1:0])** to 0x01 at the end of SPI memory initialization sequence to automatically trigger the mode of operation transition from **Stop (SYS_BOOT_DONE)** to **Streaming**.

The throughput of the SPI interface can be 48Mbps. The clock frequency of SCK of the SPI master port can be programmed by setting the configuration register SPI_SCK_M **(0x2300)**. The frequency equation is:

$$f_{SCLK} = f_{pll} \cdot \frac{1}{2 \cdot (SPI\_SCK\_M + 1)}$$

The variable f_{pll} is the frequency of the internal PLL clock output.

6.7.6. Manual boot configuration

The HM1246-AWD can be set to Manual Boot by setting the BOOT strap pin low. In this setting, the HM1246-AWD does not load any content automatically during the power-up sequence. The sensor initialization sequence will be programmed by the host through the I2C interface. Once all sensor initialization registers have be programmed, the host will write MODE_SELECT **(0x0100[1:0])** as the last initialization command to 0x01 to trigger a transition from Stop to Streaming mode as shown in the Power Up Sequence drawing.

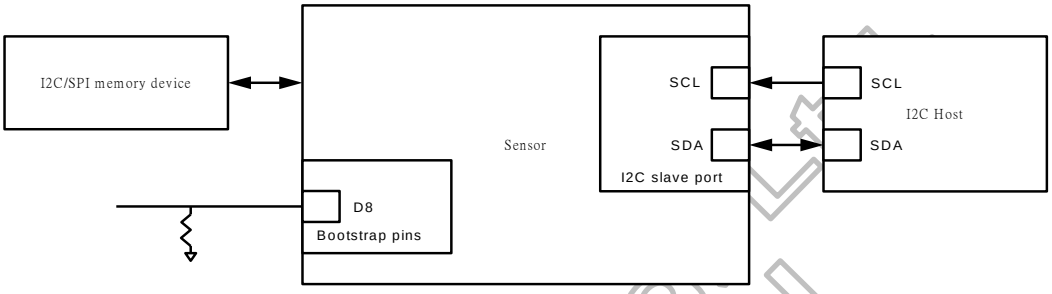


Figure 6.15: Manual boot mode connection setting

6.8. Embedded data

The HM1246-AWD support Embedded Data which contains predefined sensor register data, 16 user defined register data that can be used to load module information, and statistics. The embedded sensor register data are appended at the beginning of the frame, and the frame active period will increase by 1 row at the beginning of the frame. The frame period remains the same whether embedded data is enabled or disabled.

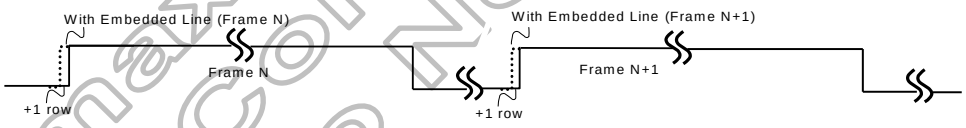


Figure 6.16: Embedded data sync fields

Both the register and statistics data are predefined, and the embedded data registers are identified in the Register Table section. Users can customize 16 register bytes for information such as module ID that will be placed at the beginning of the embedded data stream.

The embedded line data are partitioned by a programmable 8-bit Tag used to parse individual registers and statistics byte.

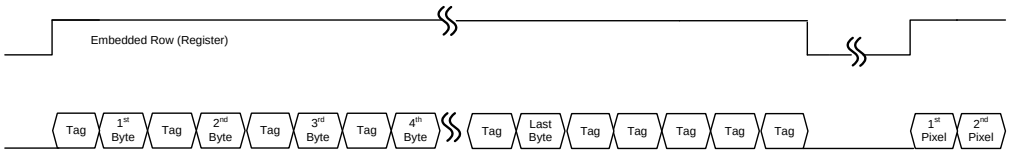


Figure 6.17: Embedded data tags

6.9. Sensor self diagnostic

The HM1246-AWD features several diagnostic and monitoring circuits to aid the system in identifying functional issues during the initialization and the operation of the sensor. The status of the embedded diagnostic and monitoring functions can be read back from the register SAFETY_FLAG **(0x7000)**, and for each event as an individually selectable option, drive the BO digital output pin. This pin can be connected to the system host to serve as an interrupt function. The Status Register value can also be read through the Embedded Line. Both the Status Register and the BO pin can be cleared by reading the register SAFETY_FLAG **(0x7000)** through the I2C interface.

Event	Enabling event	Configuration field	Status register	BO pin enable
I2C data load CRC-16 error	I2C_CRC_ERR	Always enabled	0x7000[0]	0x7001[0]
SPI data load CRC-16 error	SPI_CRC_ERR	Always enabled	0x7000[1]	0x7001[1]
Test pattern CRC-16 error	TEST_PTRN_ERR	ASIL_TEST_PTRN_EN **(0x2003[1])**	0x7000[2]	0x7001[2]
SRAM BIST error	BIST_ERR	Always enabled	0x7000[3]	0x7001[3]
AVDD brown-out	AVDD_BO	AVDD_BO_EN **(0x5220[4])**	0x7000[4]	0x7001[4]
Temperature out-of-range	TEMP_ERR	Always enabled	0x7000[5]	0x7001[5]

Table 6.9: Sensor system error notification event and registers

6.9.1. Data port link integrity

The sensor contains a checksum generator to calculate the polynomial of $x^{16}+x^{12}+x^5+1$ 16-bit checksum of each video frame. The CRC-16 checksum generator shall shift in 10/8 bit **(MSB first)** of the data port output and calculate the 16-bit checksum every clock cycle according to the table below. At the end of the frame, the checksum value can be read from registers 0x7009 and 0x700A, and from the Embedded Line.

Mode of operation	Data port width	CRC-16 input format
10-bit ADC RAW	10-bit	DP[9:0]
10-bit ADC YUV, RGB	8-bit	DP[7:0]

Table 6.10: Data link CRC16

6.9.2. External memory port link integrity

When sensor receives data from external memory devices, a CRC-16 checksum with polynomial of $x^{16}+x^{15}+x^2+1$ is computed. After receiving the EOF byte, the sensor will compare the subsequent 2-byte checksum with the calculated checksum value, and send the error flag value **(0: same – pass; 1: different – fail)** to the register and the Embedded Line. Should the CRC value from the SPI or I2C not match with the CRC value stored in the respective external memory, the register bit SPI_CRC_ERR_FLAG **(0x7000[1])** or the register bit I2C_CRC_ERR_FLAG **(0x7000[0])** will be set high, respectively.

6.9.3. Test pattern test

The sensor can perform an optional raw data test pattern test during boot up. The test pattern is predefined in the sensor and the Black Level Correction, Cropping, Static Defect Pixel Detection and Lens Shading Correction shall be disabled automatically.

Once the sensor completes the transmission of the test pattern image, the sensor will compare the calculated CRC-16 checksum with the configuration register bits TST_PTRN_CRC[15:0] {0x7004, 0x7005} and send the TEST_PTRN_ERR_FLAG value **(0: match – pass; 1: not matched – fail)** to the Embedded Line. A read-only configuration register bit TEST_PTRN_ERR_FLAG **(0x7000[2])** will store the result of test pattern CRC-16 result **(1: fail; 0: pass)**. The calculated CRC-16 checksum value can be read through the I2C slave interface.

6.9.4. Internal SRAM built in self test

The SRAM memory of the sensor is supported with a Built-In Self Test engine to identify SRAM address decoder faults, stuck-at faults, transition faults and coupling faults during each power up. The test status of the SRAM BIST can be read through the register bits SRAM_BIST_STATUS **(0x7003[1:0])**. The result will be shown in register bit SRAM_BIST_ERR_FLAG **(0x7000[3])** and can also be read in the Embedded Line.

6.9.5. Voltage brown out

The Voltage Brown Out circuit monitors the AVDD voltage which supplies power to the pixel array and analog circuits. When the AVDD supply sags below a programmed threshold, the AVDD_BO event will be triggered and set register bit AVDD_BO_FLAG **(0x7000[4])** to 1.

When AVDD_BO event occurs, the internal hardware that triggers AVDD_BO flag shall be disabled so it does not trigger when the same event happens again. The configuration register bit AVDD_BO_ARM **(0x7008[2])** has to be set to reset the internal hardware that triggers AVDD_BO.

The AVDD_BO event can be programmed to set the video output to 0, while the sensor continues to operate. The option is enabled by setting register bit AVDD_BO_ZERO_OUT **(0x7008[1])** to 1.

6.9.6. Temperature Out-of-Range

The HM1246-AWD features a 7-bit temperature sensor which is internally updated every frame. When the temperature sensor reading is outside the range between the configuration register bits MAX_TEMP **(0x7006[6:0])** and MIN_TEMP **(0x7007[6:0])**, the read-only configuration register bit TEMP_ERR_FLAG **(0x7000[5])** and the Embedded Line field TEMP_FLAG shall be set.

7. Serial Interface Description

7.1. I2C bus

The 2-Wire serial interface provides read/write access to the sensor registers

- 2-Wire serial interface consists of SDA **(bidirectional serial data)** and SCL **(serial clock)** pins.
- HM1246-AWD uses 16-bit register address and 8-bit register data.
- The sensor uses double-buffered registers to ensure that register changes that affect sensor operation takes place at the beginning of the next valid video frame.
- The host generates SCL clock signal to the sensor and uses the signal to synchronize all data transfer.

7.1.1. Slave address

- If the configuration register bit I2C_ID_SEL **(0x2200[0])** is 0, slave address is configured by D1 and D0 pins following the table below. This option is the default setting.
- If the configuration register bit I2C_ID_SEL **(0x2200[0])** is 1, slave address is assigned to a 7-bit value by setting the configuration register bits I2C_ID **(0x2201[6:0])**
- These configuration register settings are set by the commands stored in OTP or SPI/I2C external memory device.

D1	D0	Address
Pull Down	Pull Down	0x24 **(7-bit)**
Pull Down	Pull Up	0x25 **(7-bit)**
Pull Up	Pull Down	0x34 **(7-bit)**
Pull Up	Pull Up	0x35 **(7-bit)**

Table 7.1: Device address configuration

7.1.2. Start / Stop conditions

The Start and Stop conditions on the serial bus is issued by the Host.

SDA Transition	SCL	Condition
High to Low	High	Start
Low to High	High	Stop

Table 7.2: Serial interface Start / Stop transition

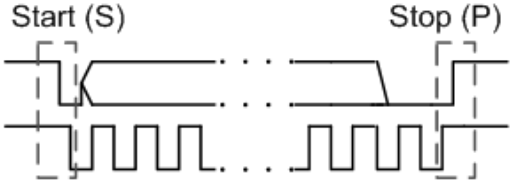


Figure 7.1: 2-Wire serial interface Start / Stop condition

7.1.3. Data valid

One SCL pulse is generated for each data bit transferred. The host should ensure that the SDA signal must be stable when SCL in High. The SDA signal can transition when SCL is Low.

7.1.4. Data format

Data is transferred one byte at a time. The most significant bit should always be transferred first. Each byte is followed by an Acknowledge **(ACK)** or a No-Acknowledge bit **(No ACK)**.

7.1.5. Acknowledge / No-Acknowledge

Each 8-bit is followed by an Acknowledge **(ACK)** or No-Acknowledge **(No ACK)** bit.

- Acknowledge: The Host will release the SDA line. The sensor will drive the SDA line low.
- No-Acknowledge: The Host will release the SDA line. The sensor will not drive the SDA pin **(Pulled high)**. The No ACK bit is used to terminate a read sequence.

7.1.6. Write sequence

- Initiated by Host with Start **(S)** condition, followed by 8-bit device slave ID **(write ID)**
- If the slave ID is recognized by the sensor, the ACK bit will be sent to the Host.
- Once the Host receives an ACK from the sensor, it can begin to transmit the register address **(high byte first, then low byte)**, then the register data. After each byte, the sensor will issue an ACK or No ACK signal.
- The write operation is completed when the Host asserts a stop condition

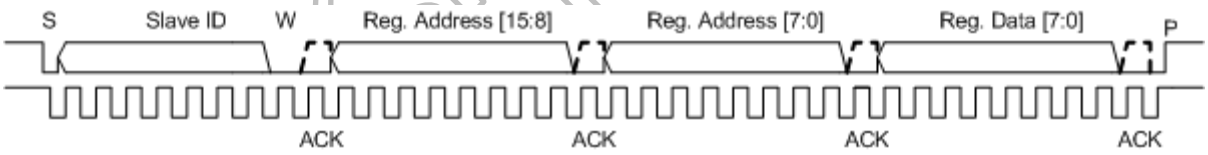


Figure 7.2: 2-Wire serial interface 16-bit address write

7.1.7. Read sequence

- Initiated by Host with Start **(S)** condition, followed by the 8-bit device slave ID **(write ID)**.
- If the slave ID is recognized by the sensor, the ACK bit will be sent to the Host.
- Once the Host receives an ACK from the sensor, it can begin to transmit the register address **(high byte first, then low byte)**, then the register data. After each byte, the sensor will issue an ACK or No ACK bit.
- The write operation is completed when the Host asserts a Stop condition.
- The Host must issue another Start condition, followed by the 8-bit device slave ID **(Read ID)**.
- If the register ID is recognized by the sensor, the ACK bit will be sent to the Host.
- The sensor will respond with the Register Data Out.
- The Host will issue an ACK, and then asserts the Stop condition.

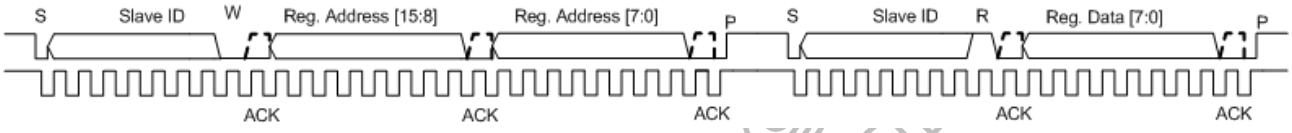


Figure 7.3: 2-Wire serial interface 16-bit address read

7.1.8. Burst sequence

The HM1246-AWD supports multi-byte registers access through I2C burst read and write operation. The host specifies the header **(one ID byte and two address bytes)** after which the sensor will automatically increment the address for every data byte access.

8. Sensor Control

8.1. Trigger control

Frame can be triggered for either multiple frames or single snapshot by setting register bit MODE_SELECT **(0x0100[1:0]=0x01)**.

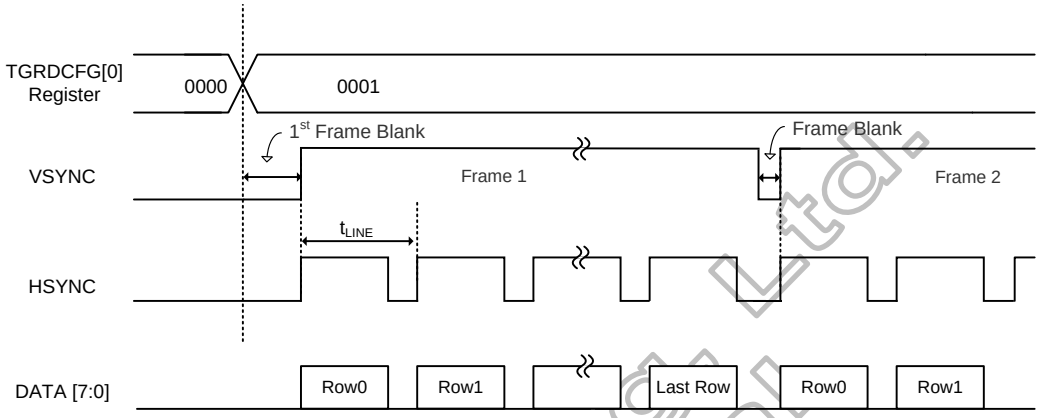


Figure 8.1: Rolling shutter vs. continuous frame

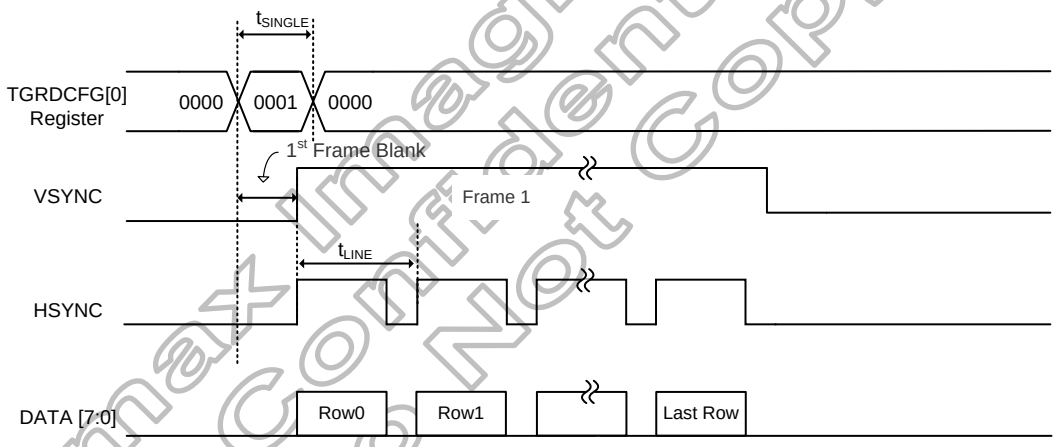


Figure 8.2: Rolling shutter vs. single frame

8.2. Exposure control

The sensor supports coarse integration control with a programmable resolution of 1 row. The exposure time of the sensor is calculated using the following equation:

A. ***Integration time (seconds) = coarse_integration x line_length_pck / vt_pix_clk (MHz) x 1 x 10^6***
Minimum integration row = 4
Maximum integration time = coarse_integration_time ≤ (frame_length_lines – 2)
If this limit is not applied, the frame time will automatically be extended to (coarse_integration_time + 2) to accommodate the larger integration time.

8.2.1. 50Hz / 60Hz flicker avoidance

The sensor integration time should be set in intervals of 1/100 seconds or 1/120 seconds for 50Hz / 60Hz flicker avoidance, respectively.

A. ***Integration Step Size (60Hz Avoidance) = vt_pix_clk (MHz) x 1 x 10^6 / line_length_pck / 120***
B. ***Integration Step Size (50Hz Avoidance) = vt_pix_clk (MHz) x 1 x 10^6 / line_length_pck / 100***

8.3. Frame rate control

8.3.1. Full frame readout

In full frame readout mode, the frame rate of the sensor is calculated using the following equations:

A. ***4096 ≥ line_length_pck ≥ min_line_length_pck***
B. ***65535 ≥ frame_length_lines ≥ min_frame_length_lines***
C. ***If coarse_integration > frame_length_lines - 2, then***
frame rate = vt_pix_clk MHz x 1 x 10^6 / (coarse_integration x line_length_pck)
else,
frame rate = vt_pix_clk MHz x 1 x 10^6 / (frame_length_lines x line_length_pck)

8.3.2. Sub2 frame readout

In sub2 frame readout mode **(skip, bin)**, the frame rate of the sensor is calculated using the following equations:

A. ***4096 ≥ line_length_pck ≥ min_line_length_pck***
B. ***65535 ≥ frame_length_lines ≥ min_frame_length_lines***
C. ***If coarse_integration ≤ frame_length_lines - 2, then frame rate = vt_pix_clk MHz x 1 x 10^6 / (frame_length_lines x line_length_pck)***
else
frame rate = vt_pix_clk MHz x 1 x 10^6 / (coarse_integration x line_length_pck)

8.4. Analog gain control

The global analog gain based on the following equation:

Analog gain = X = (ANALOG_GLOBAL_GAIN [7:0] + 16) / 16

X (Hex)	Gain (x)	Gain (dB)	X (Hex)	Gain (x)	Gain (dB)
0x00	1	0.0	0x30	4	12.0
0x01	1.0625	0.5	0x34	4.25	12.6
0x02	1.125	1.0	0x38	4.5	13.1
0x03	1.1875	1.5	0x3C	4.75	13.5
0x04	1.25	1.9	0x40	5	14.0
0x05	1.3125	2.4	0x44	5.25	14.4
0x06	1.375	2.8	0x48	5.5	14.8
0x07	1.4375	3.2	0x4C	5.75	15.2
0x08	1.5	3.5	0x50	6	15.6
0x09	1.5625	3.9	0x54	6.25	15.9
0x0A	1.625	4.2	0x58	6.5	16.3
0x0B	1.6875	4.5	0x5C	6.75	16.6
0x0C	1.75	4.9	0x60	7	16.9
0x0D	1.8125	5.2	0x64	7.25	17.2
0x0E	1.875	5.5	0x68	7.5	17.5
0x0F	1.9375	5.7	0x6C	7.75	17.8
0x10	2	6.0	0x70	8	18.1
0x12	2.125	6.5	0x78	8.5	18.6
0x14	2.25	7.0	0x80	9	19.1
0x16	2.375	7.5	0x88	9.5	19.6
0x18	2.5	8.0	0x90	10	20.0
0x1A	2.625	8.4	0x98	10.5	20.4
0x1C	2.75	8.8	0xA0	11	20.8
0x1E	2.875	9.2	0xA8	11.5	21.2
0x20	3	9.5	0xB0	12	21.6
0x22	3.125	9.9	0xB8	12.5	21.9
0x24	3.25	10.2	0xC0	13	22.3
0x26	3.375	10.6	0xC8	13.5	22.6
0x28	3.5	10.9	0xD0	14	22.9
0x2A	3.625	11.2	0xD8	14.5	23.2
0x2C	3.75	11.5	0xE0	15	23.5
0x2E	3.875	11.8	0xE8	15.5	23.8

Table 8.1: Global analog gain settings

8.5. Frame retiming

Serial registers that are synchronized to sensor timing utilize double-buffer register to ensure that changes take effect at the start of a subsequent frame. The registers that require Command Update registers, such as integration and gain, are indicated by the type designator **CMU**.

The sequence is as follows:

- User writes to the target serial register**(s)** where the value**(s)** will be stored in the first buffer.
- User issues Command Update **(CMU)** by writing any non-zero value to register 0x0104. The register values will be moved to the second register buffer
- If the double-buffer registers and CMU are issued before frame trigger, the first frame **(Frame N)** will apply the new values.
- If the CMU is issued after the frame trigger, the first frame using the new settings will be Frame N+2. The settings for Frame N+1 may use the current settings or new settings depending on the CMU relative to the internal start of the next frame.
- Note there are no bad frames such that two settings may be applied to a single frame. Should the new setting be applied to Frame N+2, then Frame N+1 would simply use the previous settings.

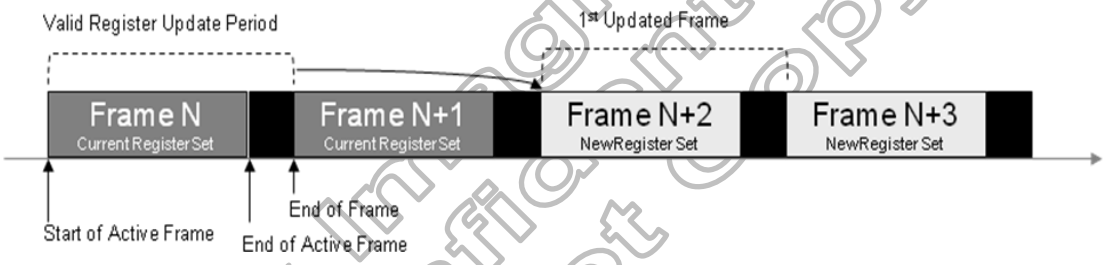


Figure 8.3: (N+2) command update timing

9. Video Output Format and Control

9.1. Parallel interface

The HM1246-AWD supports RAW10, YCbCr, RGB 565 / 555 / 444. The data format is select through register bit OUTPUT_PRT_CTRL **(0x2F02)**.

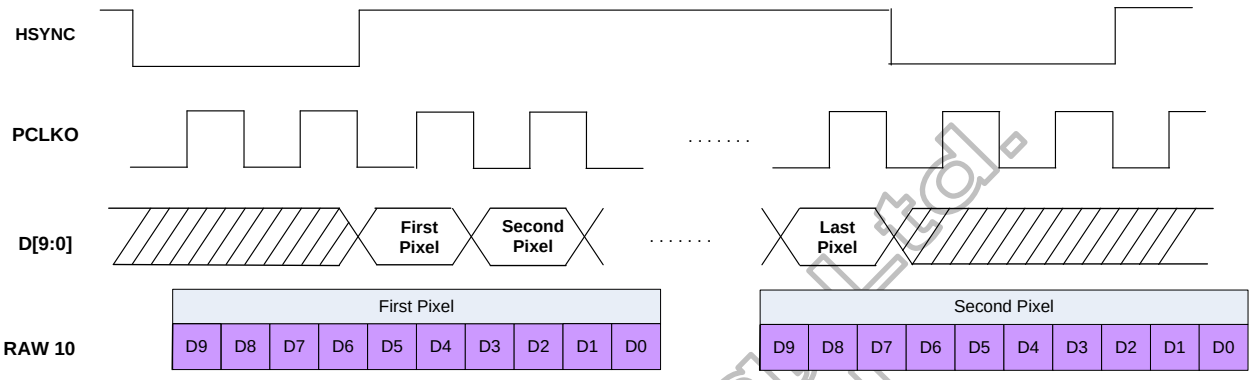


Figure 9.1: RAW output format

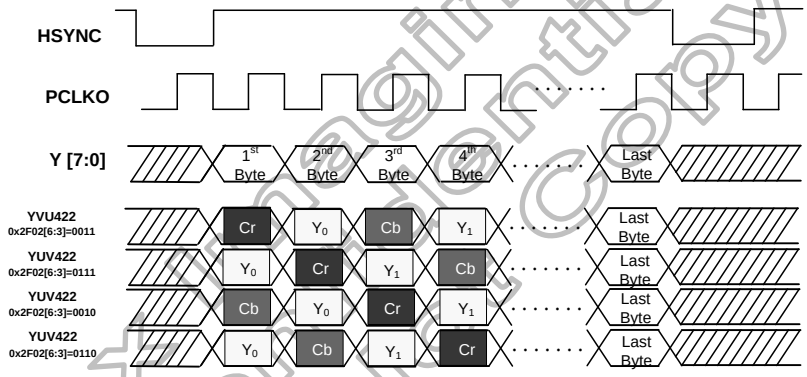


Figure 9.2: YCbCr output format

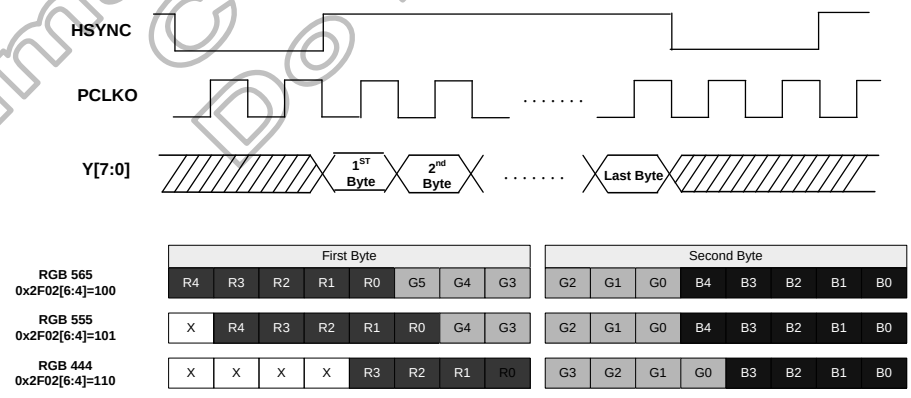


Figure 9.3: RGB 565 / 555 /444 output format

The HM1246-AWD supports synchronization method of CCIR656. When enabling the CCIR656 mode **(0x2F06=0x88)**, synchronization codes are embedded in the output data and HSYNC / VSYNC won't be output. In this mode, EAV and SAV are outputting SYNC codes as listed in Table 9.1: The definition of CCIR656 embedded synchronization code.

Name	Description	4-bytes sequence
SAV	Line start	FF 00 00 80
EAV	Line end	FF 00 00 9D
SAV **(blanking)**	Line start **(VSYNC blanking)**	FF 00 00 AB
EAV **(blanking)**	Line end **(VSYNC blanking)**	FF 00 00 B6

Table 9.1: The definition of CCIR656 embedded synchronization code

9.2. IO control

9.2.1. Output enable

When not in use, the I/O pins can be tri-stated allowing multiple devices to share the same bus by pulling low the “XSHUTDOWN” pin. When normal operating, I/O pins will be tri-stated if not be used. The IO drive strength and slew rate are also can be configured to meet the system requirements.

Pad name	Strength (3-bit control)	Slew rate control (3-bit control)	Output enable	H/W XSHUTDWON mode
D8 ~ D9	IOPADTOP1 **(0x5229[4:2])**	IOPADTOP1 **(0x5229[7:5])**	0x2F02[6:4]=0x02	HiZ
D0 ~ D7			ACTIVE	HiZ
PCLKO	IOPADTOP2 **(0x522A[2:0])**	IOPADTOP2 **(0x522A[5:3])**	ACTIVE	HiZ
HSYNC	IOPADTOP1 **(0x5229[4:2])**	IOPADTOP1 **(0x5229[7:5])**	ACTIVE	HiZ
VSYNC			ACTIVE	HiZ
LED_OUT			0x5400[2:0]=0x00	HiZ
GPIO2			0x5400[1:0]=0x00	HiZ
GPIO1			0x5400[1:0]=0x00	HiZ
BO			Always	HiZ
SDO_SDA	IOPADTOP3 **(0x522B[2:0])**	IOPADTOP3 **(0x522B[5:3])**	0x2001[3:2]=0x02 & 0x2F03[3]=0x00 or 0x2001[3:2]=0x01	HiZ
SCK_SCL				HiZ
SCS			0x2001[3:2]=0x02 & 0x2F03[3]=0x00	HiZ

Table 9.2: Output control table

9.2.2. IO control

The IO drive current and polarity can be configured to meet a wide array of system requirements. The IO signals are synchronized to the PCLKO output. By default, the data signal transitions on the falling edge of PCLKO. This allows the user to latch data on the subsequent rising edge of PCLKO.

IO pad	Polarity control	Default polarity
PCLKO	0x2F24[3]	Data transition on falling edge
VSYNC	0x2F20[6]	Active High
HSYNC	0x2F20[7]	Active High

Table 9.3: IO control

10. Register Table

- There are 3 types of registers, Read-Write **(RW)**, Read-Only **(RO)** and Write-Only **(WO)** registers.
- Registers that require Command Update are indicated by **CMU**.
- Registers embedded in embedded data line are indicated by **EM**.
- Writing to reserved and unlisted registers will cause undefined sensor behavior.
- All default settings are indicated in bold.

Command update

Serial registers that are synchronized to sensor timing utilize double-buffer register to ensure that changes take effect at the start of a subsequent frame. In the Register Table section of this document, the registers that require Command Update, such as integration and gain, are indicated by the **CMU** column

The sequence is as follows:

- User writes to the target serial register**(s)** where the value**(s)** will be stored in the first buffer.
- User issues Command Update **(CMU)** by writing one value to register 0x0104. The register values will be moved to the second register buffer
- If the double-buffer registers and CMU are issued during the active period of Nth frame, the frame N+2 will apply the new value

10.1. Status registers [0x0000 – 0x0006]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x0000	[7:0]	MODEL_ID_H	RO	16-bit sensor Part number	Y	-	0x12
0x0001	[7:0]	MODEL_ID_L			Y	-	0x45
0x0002	[7:0]	SILICON_REV	RO	Silicon Revision Number	Y	-	Note(1)
0x0005	[7:0]	FRAME_COUNT	RO	8-bit frame counter value; reset to 0xFF during SW Standby	Y	-	0xFF
0x0006	[1:0]	PIXEL_ORDER	RO	[1:0]: Color Pixel Order 00: GR 01: RG 10: BG 11: GB	-	-	0x02

Note: (1) Please consult with Himax Imaging.

10.2. General setup registers [0x0100 – 0x0110]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x0100	[1:0]	MODE_SELECT	RW	[1:0]: Sensor mode selection 00: SW standby mode 01: Streaming mode 10: Stop mode	-	Y	0x02
0x0101	[1:0]	IMAGE_ORIENTATION	RW	Image Orientation [1]:Vertical flip En [0]:Horizontal mirror En	Y	Y	0x00
0x0102	[0]	EM_DATA_EN	RW	[0]: Embedded data enable 0: Disable 1: Enable	-	Y	0x00
0x0103	[0]	SW_RESET	WO	Software Reset	-	-	-
0x0104	[0]	CMU_UPDATE	WO	CMU update	-	-	-
0x0105	[1:0]	CMU_UPDATE_AWB	WO	CMU update for AWB Gain	-	Y	-
0x0110	[7:0]	EMBEDDED_TAG	RW	TAG for embedded content	Y	-	0x5A

10.3. Output setup registers [0x0202 – 0x020F]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x0202	[7:0]	COARSE_INTG_H	RW	Coarse integration time in lines **(16-bit UINT)**	Y	Y	0x01
0x0203	[7:0]	COARSE_INTG_L	RW		Y	Y	0x08
0x0205	[7:0]	ANALOG_GLOBAL_GAIN	RW	Analog Global Gain code	Y	Y	0x00
0x0206	[2:0]	CHANNELGAIN_GR_H	RW	Channel Gain Gr code **(3.6 fixed point number, 3 integer bits 0x0206[2:0], 6 fractional bits 0x0207[7:2])**	Y	Y	0x01
0x0207	[7:2]	CHANNELGAIN_GR_L	RW		Y	Y	0x00
0x0208	[2:0]	CHANNELGAIN_R_H	RW	Channel Gain R code **(3.6 fixed point number, 3 integer bits 0x0208[2:0], 6 fractional bits 0x0209[7:2])**	Y	Y	0x01
0x0209	[7:2]	CHANNELGAIN_R_L	RW		Y	Y	0x00
0x020A	[2:0]	CHANNELGAIN_B_H	RW	Channel Gain B code **(3.6 fixed point number, 3 integer bits 0x020A[2:0], 6 fractional bits 0x020B[7:2])**	Y	Y	0x01
0x020B	[7:2]	CHANNELGAIN_B_L	RW		Y	Y	0x00
0x020C	[2:0]	CHANNELGAIN_GB_H	RW	Channel Gain Gb code **(3.6 fixed point number, 3 integer bits 0x020C[2:0], 6 fractional bits 0x020D[7:2])**	Y	Y	0x01
0x020D	[7:2]	CHANNELGAIN_GB_L	RW		Y	Y	0x00
0x020E	[1:0]	DIGITAL_GLOBAL_GAIN_H	RW	Digital Global Gain code **(2.6 fixed point number, 2 integer bits 0x020E[1:0], 6 fractional bits 0x020F[7:2])**	Y	Y	0x01
0x020F	[7:0]	DIGITAL_GLOBAL_GAIN_L	RW		Y	Y	0x00

10.4. Clock setup registers [0x0303 – 0x030D]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x0303	[7:0]	PLL1CFG	RW	PLL_MUTIPLIER_D[7:0]	-	-	0xAF
0x0305	[5:0]	PLL2CFG	RW	PLL_MUTIPLIER_D: [5:1]: pll_clk_div_d [0]: PLL_MUTIPLIER_D[8] Pre PLL CLK Divider:	-	-	0x1A
0x0307	[7:0]	PLL3CFG	RW	Vt_sys_div_d[7:0]	-	-	0x34
0x030B	[2:0]	PLL5CFG	RW	[2:0]: Vt_sys2_div_d	-	-	0xAF
0x030D	[5] [1]	PLL6CFG	RW	[5]: pll_post_div_2_d [1]: fraction_div_d	-	-	0x1A

10.5. Frame timing registers [0x0340 – 0x0343]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x0340	[7:0]	FRAME_LENGTH_LINES_H	RW	frame_length_lines **(the frame length should be greater than 18) (16-bit UINT)**	Y	Y	0x03
0x0341	[7:0]	FRAME_LENGTH_LINES_L	RW		Y	Y	0xDE
0x0342	[7:0]	LINE_LENGTH_PCK_H	RW	line_length_pck **(the line length should be less than 0x1000) (16-bit UINT)**	Y	Y	0x05
0x0343	[7:0]	LINE_LENGTH_PCK_L	RW		Y	Y	0x84

10.6. Image size registers [0x0344 – 0x0358]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x0344	[3:0]	X_ADDR_START_H	RW	x_addr_start **(12-bit UINT)**	-	Y	0x00
0x0345	[7:0]	X_ADDR_START_L	RW		-	Y	0x00
0x0346	[3:0]	Y_ADDR_START_H	RW	y_addr_start **(12-bit UINT)**	-	Y	0x00
0x0347	[7:0]	Y_ADDR_START_L	RW		-	Y	0x00
0x0348	[3:0]	X_ADDR_END_H	RW	x_addr_end **(12-bit UINT)**	-	Y	0x05
0x0349	[7:0]	X_ADDR_END_L	RW		-	Y	0x0F
0x034A	[3:0]	Y_ADDR_END_H	RW	y_addr_end **(12-bit UINT)**	-	Y	0x03
0x034B	[7:0]	Y_ADDR_END_L	RW		-	Y	0xCF
0x0351	[7:0]	X_LA_START_H	RW	The first window X Start **(High Byte)**	-	Y	0x00
0x0352	[7:0]	X_LA_START_L	RW	The first window X Start **(Low Byte)**	-	Y	0x3C
0x0353	[7:0]	X_LA_END_H	RW	The first window X End **(High Byte)**	-	Y	0x05
0x0354	[7:0]	X_LA_END_L	RW	The first window X End **(Low Byte)**	-	Y	0x4B
0x0355	[7:0]	Y_LA_START_H	RW	The first window Y Start **(High Byte)**	-	Y	0x00
0x0356	[7:0]	Y_LA_START_L	RW	The first window Y Start **(Low Byte)**	-	Y	0x00
0x0357	[7:0]	Y_LA_END_H	RW	The first window Y End **(High Byte)**	-	Y	0x03
0x0358	[7:0]	Y_LA_END_L	RW	The first window Y End **(Low Byte)**	-	Y	0xCF

10.7. Sub-sampling registers [0x0383 – 0x0387]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x0383	[3:0]	X_SUB_EN	RW	x_odd_increment [3:0] 0001: Full 0011: Sub2 Others: Invalid	Y	Y	0x01
0x0387	[3:0]	Y_SUB_EN	RW	y_odd_increment [3:0] 0001: Full 0011: Sub2 Others: Invalid	Y	Y	0x01

10.8. Binning mode registers [0x0390]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x0390	[4] [2:0]	BINNING_MODE	RW	[4]: Resampling Enable [2]: Digital Summing [1]: Horizontal Binning [0]: Vertical Binning	Y	Y	0x00

10.9. Test pattern registers [0x0601 – 0x0609]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x0601	[7:0]	TEST_PATTERN_MODE	RW	Test Pattern Mode [7:4]: 0000: B & W square 0001: Gray blending 0010: Walking 01 0011: Color bar blending 0100: Color bar 0101 R color blending **(6)** 0110: R color blending **(25)** 0111: R color blending **(50)** 1000: G color blending **(6)** 1001: G color blending **(25)** 1010: G color blending **(50)** 1011: B color blending **(6)** 1100: B color blending **(25)** 1101: B color blending **(50)** 1110: Value 512 1111: Solid Color [3:1]: Reserved [0]: Test Pattern enable	Y	Y	0x00
0x0602	[4:0]	TEST_DATA_BLUE_H	RW	Test data BLUE **(13-bit UINT)**	-	-	0x00
0x0603	[7:0]	TEST_DATA_BLUE_L	RW		-	-	0x00
0x0604	[4:0]	TEST_DATA_GB_H	RW	Test data greenB **(13-bit UINT)**	-	-	0x00
0x0605	[7:0]	TEST_DATA_GB_L	RW		-	-	0x00
0x0606	[4:0]	TEST_DATA_RED_H	RW	Test data RED **(13-bit UINT)**	-	-	0x00
0x0607	[7:0]	TEST_DATA_RED_L	RW		-	-	0x00
0x0608	[4:0]	TEST_DATA_GR_H	RW	Test data greenR **(13-bit UINT)**	-	-	0x00
0x0609	[7:0]	TEST_DATA_GR_L	RW		-	-	0x00

10.10. SBC registers [0x2000 – 0x2009]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x2000	[7:0]	BOOT_REF1	RW	[7]: MEM_SIZE **(R/O)** [6]: BOOT **(R/O)** [5]: Reserved [4]: MIRROR **(R/O)** [3:2]: FLICKER[1:0] [1]: sampled FLIP **(R/O)** [0]: B_AND_W	Y	-	0x40
0x2001	[4:0]	BOOT_REF2	RO	[4]: PLL_LOCK [3:2]: MEM_CFG[1:0] [1:0]: I2CID_LSB[1:0]	-	-	0x00
0x2002	[4:0]	SBP	RW	[4]: Reserved [3]: MIRROR_SBP [2]: FLK_SBP [1]: FLIP_SBP [0]: BW_SBP	-	-	0x1F
0x2003	[1:0]	SBC_CTRL	RW	[1]: ASIL_TEST_PTRN_EN ASIL test pattern control; active high. [0]: PLL_EN: PLL control; active high.	-	-	0x00
0x2004	[3:0]	DELAY_VALUE_H	RW	[3:0]: DELAY_VALUE[19:16]	-	-	0x00
0x2005	[7:0]	DELAY_VALUE_M	RW	[7:0]: DELAY_VALUE[15:8]	-	-	0x00
0x2006	[7:0]	DELAY_VALUE_L	RW	[7:0]: DELAY_VALUE[7:0]	-	-	0x00
0x2008	[4:0]	OTP_BYTE_CNT_H	RO	[4:0]: OTP_BYTE_CNT[12:8]	Y	-	0x00
0x2009	[7:0]	OTP_BYTE_CNT_L	RO	[7:0]: OTP_BYTE_CNT[7:0]	Y	-	0x02

10.11. I2C master control registers [0x2100 – 0x2101]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x2100	[7:0]	I2C_CLK_M	RW	Determine the SCL frequency of the master I2C interface. [7:0]: I2C_CLK_M[7:0] I2C_CLK frequency = system clock frequency / (2*(1+I2C_CLK_M))	-	-	0x95
0x2101	[6:0]	EXT_I2C_DEV_ID	RW	Assign the default I2C ID of the external I2C device. [6:0]: EXT_I2C_DEV_ID[6:0]	-	-	0x50

10.12. I2C slave control registers [0x2200 – 0x2206]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x2200	[0]	I2C_ID_SEL	RW	[0]: I2C_ID_SEL selects bootstrap pin sampled value vs. I2C_ID[6:0] configuration field as the I2C ID of device. 0: I2C ID = {2'b01, I2CID[1], 3'b010, I2CID[0]} where I2CID[1:0] are the sampled bootstrap pin values. 1: Device I2C ID = the configuration field I2C_ID[6:0].	-	-	0x00
0x2201	[6:0]	I2C_ID	RW	[6:0]: I2C_ID[6:0] is the configuration field that assigns device I2C ID when I2C_ID_SEL=1	-	-	0x30
0x2202	[0]	I2C_ACC_SPI	RW	[0]: I2C_ACC_SPI: SPI access starts when this bit is set. I2C_ACC_SPI is automatically cleared when the SPI access is finished.	-	-	0x00
0x2203	[0]	SPI_WRITE_LENGTH_H	RW	[0]: SPI_WRITE_LENGTH[8]	-	-	0x00
0x2204	[7:0]	SPI_WRITE_LENGTH_L	RW	[7:0]: SPI_WRITE_LENGTH[7:0]	-	-	0x00
0x2205	[0]	SPI_READ_LENGTH_H	RW	[0]: SPI_READ_LENGTH[8]	-	-	0x00
0x2206	[7:0]	SPI_READ_LENGTH_L	RW	[7:0]: SPI_READ_LENGTH[7:0]	-	-	0x00

10.13. SPI control registers [0x2300 – 0x2302]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x2300	[7:0]	SPI_SCK_M	RW	[7:0]: SPI_SCK_M[7:0] SPI_SCK frequency = PLL_CLK frequency / (2 * (1+SPI_SCK_M))	-	-	0x04
0x2302	[7:0]	BUF8K_WP	RW	[7:0]: BUF8K_WP[7:0] SPI-OSD buffer write protection; BUF8K_WP = 0xB8 to unlock the write protection	-	-	0x00

10.14. OTP registers [0x2500 – 0x25FF]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x2500	[2:0]	OTP_PAGE	RW	OTP page number; valid range	-	-	0x00
0x2501	[5:0]	OTP_OFFSET	RW	OTP page offset	-	-	0x00
0x2502	[6:0]	OTP_LENGTH	RW	OTP length	-	-	0x40
0x2503	[2:0]	OTP_CMD	RW	OTP command register [2]: OTP Program Mode 0: OTP HV Disable 1: OTP HV Enable [1:0]: User Program Mode 00: Idle 01: Write from user space to OTP 10: Read from OTP to user space	-	-	0x00
0x2504	[1:0]	OTP_STATUS	RO	OTP Read / Write Status [1]: Write Busy [0]: Read Busy	-	-	0x00
0x2519	[7:0]	OTP_PWE_PULSE_INTERVAL_H	RW	Timing counter for Write Pulse Interval Timing configuration	-	-	0x00
0x251A	[7:0]	OTP_PWE_PULSE_INTERVAL_L	RW	Timing counter for Write Pulse Interval Timing configuration	-	-	0x30
0x251B	[7:0]	OTP_PWE_PULSE_WIDTH_H	RW	Timing counter for Write Pulse Width Timing configuration	-	-	0x04
0x251C	[7:0]	OTP_PWE_PULSE_WIDTH_L	RW	Timing counter for Write Pulse Width Timing configuration	-	-	0x04
0x251D	[7:0]	OTP_PRD_INTERVAL_WIDTH	RW	Timing counter for Read Pulse Interval Timing configuration	-	-	0x0E
0x251E	[7:0]	OTP_PRD_WIDTH	RW	Timing counter for Read Pulse Width Timing configuration	-	-	0x0A
0x25C0	[7:0]	OTP_USER_BYTE0	RW	OTP user data 0	-	-	-
0x25C1	[7:0]	OTP_USER_BYTE1	RW	OTP user data 1	-	-	-
				:			
0x25FF	[7:0]	OTP_USER_BYTE63	RW	OTP user data 63	-	-	-

10.15. System registers [0x2F01 – 0x2F24]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x2F01	[7]	CKCFG	RW	[7]: digital clock source selection 0: PLL 1: System clock	-	-	0x00
0x2F02	[7:0]	OUTPUT_PRT_CTRL	RW	Output Control [7]: ITU 601 enable [6:4]: Data Type Selection 001: YUV422 **(UV first)** 010: Raw output 011: YUV422 **(Y first)** 100: RGB565 101: RGB555 110: RGB444 111: Monochrome [3]: CbCr order selection 1: Cr first 0: Cb first [2]: Reserved [1:0]: Order Selection If RGB565 is selected, 10: Byte1: {B[3:7], G[2:4]}, Byte2: {G[5:7], R[3:7]} 00, 01, 11: Byte1: {R[7:3], G[7:5]}, Byte2: {G[4:2], B[7:3]} If RGB555 is selected, 01: Byte1: {B[7:3], G[7:5]}, Byte2: {G[4:3], 1'b0, B[7:3]} 10: Byte1: {B[3:7], 1'b0, G[3:4]}, Byte2: {G[5:7], R[3:7]} 00, 11: Byte1 {1'b0, R[7:3], G[7:6]}, Byte2: {G[5:3], B[7:3]} If RGB444 is selected, 01: Byte1: {R[7:4], 1'b1, G[7:5]}, Byte2: {G[4], 2'b10, B[7:4], 1'b1} 10: Byte1: {1'b1, B[4:7], 2'b01, G[4]}, Byte2: {G[5:7], 1'b1, R[4:7]} 00, 11: Byte1: {4'b0, R[7:4]}, Byte2: {G[7:4], B[7:4]}	-	-	0x30
0x2F06	[7] [3]	TRC_CTRL	RW	Time-Reference Code [7]: TRC encoder enable **(CCIR656)** [3]: Aligned input Vsync/Hsync rising edge			0x00
0x2F20	[7:0]	POLARITY_CTRL	RW	[7]: HSYNC [6]: VSYNC [5:0]: Reserved	-	-	0x00
0x2F24	[4:0]	PCLK_CTRL	RW	[4]: Reserved [3]: Clock output polarity [2]: Reserved [1:0]: clock power down 11: digital clock down 00, 01, 10: digital clock on	-	-	0x00

10.16. RAW control registers [0x301C]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x301C	[7:0]	BLI_TGT	RW	[7:0]: BLI target	Y	-	0x20

10.17. Lens shading control registers [0x3030 – 0x3034]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x3030	[3:0]	LSC_CTRL	RW	[3:1]: Reserved [0]: LSC enable	-	-	0x00
0x3031	[7:0]	LSC_STR	RW	LSC strength	-	-	0x10
0x3032	[7:0]	LSC_RA_OFFSET	RW	LSC RA offset	-	-	0x00
0x3033	[7:0]	LSC_CENTERX_OFFSET	RW	LSC X center offset	-	-	0x00
0x3034	[7:0]	LSC_CENTERY_OFFSET	RW	LSC Y center offset	-	-	0x00

10.18. Resampling control registers [0x3080]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x3080	[0]	RESMP_CTRL	RW	[0]: reasmpling enable	-	-	0x01

10.19. RAW denoise registers [0x3090 – 0x30A9]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x3090	[0]	RAW_NR_EN	RW	[0]: Raw denoise enable	-	-	0x01
0x309B	[7:0]	RAW_NR_TH_B	RW	Blue raw denoise threshold 0	-	-	0x18
0x309C	[7:0]	RAW_NR_TH_B_LL	RW	Blue raw denoise threshold 1	-	-	0x0C
0x309D	[7:0]	RAW_NR_TH_B_UL	RW	Blue raw denoise threshold UL	-	-	0x28
0x309F	[7:0]	RAW_NR_TH_G	RW	G raw denoise threshold 0	-	-	0x10
0x30A0	[7:0]	RAW_NR_TH_G_LL	RW	G raw denoise threshold 1	-	-	0x0A
0x30A1	[7:0]	RAW_NR_TH_G_UL	RW	G raw denoise threshold UL	-	-	0x28
0x30A7	[7:0]	RAW_NR_TH_R	RW	R raw denoise threshold 0	-	-	0x18
0x30A8	[7:0]	RAW_NR_TH_R_LL	RW	R raw denoise threshold 1	-	-	0x0C
0x30A9	[7:0]	RAW_NR_TH_R_UL	RW	R raw denoise threshold UL	-	-	0x28

10.20. Embedded line control registers [0x3200 – 0x320F]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x3200	[7:0]	EM_USER_BYTE0	R/W	User programmable byte 0	Y	-	0x00
0x3201	[7:0]	EM_USER_BYTE1	R/W	User programmable byte 1	Y	-	0x00
0x3202	[7:0]	EM_USER_BYTE2	R/W	User programmable byte 2	Y	-	0x00
0x3203	[7:0]	EM_USER_BYTE3	R/W	User programmable byte 3	Y	-	0x00
0x3204	[7:0]	EM_USER_BYTE4	R/W	User programmable byte 4	Y	-	0x00
0x3205	[7:0]	EM_USER_BYTE5	R/W	User programmable byte 5	Y	-	0x00
0x3206	[7:0]	EM_USER_BYTE6	R/W	User programmable byte 6	Y	-	0x00
0x3207	[7:0]	EM_USER_BYTE7	R/W	User programmable byte 7	Y	-	0x00
0x3208	[7:0]	EM_USER_BYTE8	R/W	User programmable byte 8	Y	-	0x00
0x3209	[7:0]	EM_USER_BYTE9	R/W	User programmable byte 9	Y	-	0x00
0x320A	[7:0]	EM_USER_BYTE10	R/W	User programmable byte 10	Y	-	0x00
0x320B	[7:0]	EM_USER_BYTE11	R/W	User programmable byte 11	Y	-	0x00
0x320C	[7:0]	EM_USER_BYTE12	R/W	User programmable byte 12	Y	-	0x00
0x320D	[7:0]	EM_USER_BYTE13	R/W	User programmable byte 13	Y	-	0x00
0x320E	[7:0]	EM_USER_BYTE14	R/W	User programmable byte 14	Y	-	0x00
0x320F	[7:0]	EM_USER_BYTE15	R/W	User programmable byte 15	Y	-	0x00

10.21. LSC grid point gain registers [0x3420 – 0x346F]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x3420	[7:0]	grid_B_Gain_0_0	RW	grid_B_Gain_0_0_addr	-	-	0x91
0x3421	[7:0]	grid_B_Gain_1_0	RW	grid_B_Gain_1_0_addr	-	-	0x7A
0x3422	[7:0]	grid_B_Gain_2_0	RW	grid_B_Gain_2_0_addr	-	-	0x72
0x3423	[7:0]	grid_B_Gain_3_0	RW	grid_B_Gain_3_0_addr	-	-	0x83
0x3424	[7:0]	grid_B_Gain_4_0	RW	grid_B_Gain_4_0_addr	-	-	0x99
0x3425	[7:0]	grid_B_Gain_0_1	RW	grid_B_Gain_0_1_addr	-	-	0x85
0x3426	[7:0]	grid_B_Gain_1_1	RW	grid_B_Gain_1_1_addr	-	-	0x59
0x3427	[7:0]	grid_B_Gain_2_1	RW	grid_B_Gain_2_1_addr	-	-	0x49
0x3428	[7:0]	grid_B_Gain_3_1	RW	grid_B_Gain_3_1_addr	-	-	0x60
0x3429	[7:0]	grid_B_Gain_4_1	RW	grid_B_Gain_4_1_addr	-	-	0x8D
0x342A	[7:0]	grid_B_Gain_0_2	RW	grid_B_Gain_0_2_addr	-	-	0x80
0x342B	[7:0]	grid_B_Gain_1_2	RW	grid_B_Gain_1_2_addr	-	-	0x55
0x342C	[7:0]	grid_B_Gain_2_2	RW	grid_B_Gain_2_2_addr	-	-	0x44
0x342D	[7:0]	grid_B_Gain_3_2	RW	grid_B_Gain_3_2_addr	-	-	0x5C
0x342E	[7:0]	grid_B_Gain_4_2	RW	grid_B_Gain_4_2_addr	-	-	0x8D
0x342F	[7:0]	grid_B_Gain_0_3	RW	grid_B_Gain_0_3_addr	-	-	0x92
0x3430	[7:0]	grid_B_Gain_1_3	RW	grid_B_Gain_1_3_addr	-	-	0x79
0x3431	[7:0]	grid_B_Gain_2_3	RW	grid_B_Gain_2_3_addr	-	-	0x6B
0x3432	[7:0]	grid_B_Gain_3_3	RW	grid_B_Gain_3_3_addr	-	-	0x7B
0x3433	[7:0]	grid_B_Gain_4_3	RW	grid_B_Gain_4_3_addr	-	-	0x99
0x3434	[7:0]	grid_Gb_Gain_0_0	RW	grid_Gb_Gain_0_0_addr	-	-	0xAD
0x3435	[7:0]	grid_Gb_Gain_1_0	RW	grid_Gb_Gain_1_0_addr	-	-	0x8A
0x3436	[7:0]	grid_Gb_Gain_2_0	RW	grid_Gb_Gain_2_0_addr	-	-	0x7F
0x3437	[7:0]	grid_Gb_Gain_3_0	RW	grid_Gb_Gain_3_0_addr	-	-	0x96
0x3438	[7:0]	grid_Gb_Gain_4_0	RW	grid_Gb_Gain_4_0_addr	-	-	0xBC
0x3439	[7:0]	grid_Gb_Gain_0_1	RW	grid_Gb_Gain_0_1_addr	-	-	0x98
0x343A	[7:0]	grid_Gb_Gain_1_1	RW	grid_Gb_Gain_1_1_addr	-	-	0x5F
0x343B	[7:0]	grid_Gb_Gain_2_1	RW	grid_Gb_Gain_2_1_addr	-	-	0x4B
0x343C	[7:0]	grid_Gb_Gain_3_1	RW	grid_Gb_Gain_3_1_addr	-	-	0x68
0x343D	[7:0]	grid_Gb_Gain_4_1	RW	grid_Gb_Gain_4_1_addr	-	-	0xA4
0x343E	[7:0]	grid_Gb_Gain_0_2	RW	grid_Gb_Gain_0_2_addr	-	-	0x92
0x343F	[7:0]	grid_Gb_Gain_1_2	RW	grid_Gb_Gain_1_2_addr	-	-	0x59
0x3440	[7:0]	grid_Gb_Gain_2_2	RW	grid_Gb_Gain_2_2_addr	-	-	0x45
0x3441	[7:0]	grid_Gb_Gain_3_2	RW	grid_Gb_Gain_3_2_addr	-	-	0x62
0x3442	[7:0]	grid_Gb_Gain_4_2	RW	grid_Gb_Gain_4_2_addr	-	-	0xA3
0x3443	[7:0]	grid_Gb_Gain_0_3	RW	grid_Gb_Gain_0_3_addr	-	-	0xAF
0x3444	[7:0]	grid_Gb_Gain_1_3	RW	grid_Gb_Gain_1_3_addr	-	-	0x87
0x3445	[7:0]	grid_Gb_Gain_2_3	RW	grid_Gb_Gain_2_3_addr	-	-	0x76
0x3446	[7:0]	grid_Gb_Gain_3_3	RW	grid_Gb_Gain_3_3_addr	-	-	0x8A
0x3447	[7:0]	grid_Gb_Gain_4_3	RW	grid_Gb_Gain_4_3_addr	-	-	0xB8
0x3448	[7:0]	grid_Gr_Gain_0_0	RW	grid_Gr_Gain_0_0_addr	-	-	0xAC
0x3449	[7:0]	grid_Gr_Gain_1_0	RW	grid_Gr_Gain_1_0_addr	-	-	0x89
0x344A	[7:0]	grid_Gr_Gain_2_0	RW	grid_Gr_Gain_2_0_addr	-	-	0x7F
0x344B	[7:0]	grid_Gr_Gain_3_0	RW	grid_Gr_Gain_3_0_addr	-	-	0x95
0x344C	[7:0]	grid_Gr_Gain_4_0	RW	grid_Gr_Gain_4_0_addr	-	-	0xBB
0x344D	[7:0]	grid_Gr_Gain_0_1	RW	grid_Gr_Gain_0_1_addr	-	-	0x98
0x344E	[7:0]	grid_Gr_Gain_1_1	RW	grid_Gr_Gain_1_1_addr	-	-	0x5F
0x344F	[7:0]	grid_Gr_Gain_2_1	RW	grid_Gr_Gain_2_1_addr	-	-	0x4B
0x3450	[7:0]	grid_Gr_Gain_3_1	RW	grid_Gr_Gain_3_1_addr	-	-	0x67
0x3451	[7:0]	grid_Gr_Gain_4_1	RW	grid_Gr_Gain_4_1_addr	-	-	0xA3
0x3452	[7:0]	grid_Gr_Gain_0_2	RW	grid_Gr_Gain_0_2_addr	-	-	0x92
0x3453	[7:0]	grid_Gr_Gain_1_2	RW	grid_Gr_Gain_1_2_addr	-	-	0x59
0x3454	[7:0]	grid_Gr_Gain_2_2	RW	grid_Gr_Gain_2_2_addr	-	-	0x45
0x3455	[7:0]	grid_Gr_Gain_3_2	RW	grid_Gr_Gain_3_2_addr	-	-	0x62
0x3456	[7:0]	grid_Gr_Gain_4_2	RW	grid_Gr_Gain_4_2_addr	-	-	0xA2

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x3457	[7:0]	grid_Gr_Gain_0_3	RW	grid_Gr_Gain_0_3_addr	-	-	0xAF
0x3458	[7:0]	grid_Gr_Gain_1_3	RW	grid_Gr_Gain_1_3_addr	-	-	0x87
0x3459	[7:0]	grid_Gr_Gain_2_3	RW	grid_Gr_Gain_2_3_addr	-	-	0x76
0x345A	[7:0]	grid_Gr_Gain_3_3	RW	grid_Gr_Gain_3_3_addr	-	-	0x8A
0x345B	[7:0]	grid_Gr_Gain_4_3	RW	grid_Gr_Gain_4_3_addr	-	-	0xB7
0x345C	[7:0]	grid_R_Gain_0_0	RW	grid_R_Gain_0_0_addr	-	-	0x98
0x345D	[7:0]	grid_R_Gain_1_0	RW	grid_R_Gain_1_0_addr	-	-	0x85
0x345E	[7:0]	grid_R_Gain_2_0	RW	grid_R_Gain_2_0_addr	-	-	0x7C
0x345F	[7:0]	grid_R_Gain_3_0	RW	grid_R_Gain_3_0_addr	-	-	0x8D
0x3460	[7:0]	grid_R_Gain_4_0	RW	grid_R_Gain_4_0_addr	-	-	0x9F
0x3461	[7:0]	grid_R_Gain_0_1	RW	grid_R_Gain_0_1_addr	-	-	0x90
0x3462	[7:0]	grid_R_Gain_1_1	RW	grid_R_Gain_1_1_addr	-	-	0x5E
0x3463	[7:0]	grid_R_Gain_2_1	RW	grid_R_Gain_2_1_addr	-	-	0x4B
0x3464	[7:0]	grid_R_Gain_3_1	RW	grid_R_Gain_3_1_addr	-	-	0x66
0x3465	[7:0]	grid_R_Gain_4_1	RW	grid_R_Gain_4_1_addr	-	-	0x97
0x3466	[7:0]	grid_R_Gain_0_2	RW	grid_R_Gain_0_2_addr	-	-	0x8B
0x3467	[7:0]	grid_R_Gain_1_2	RW	grid_R_Gain_1_2_addr	-	-	0x59
0x3468	[7:0]	grid_R_Gain_2_2	RW	grid_R_Gain_2_2_addr	-	-	0x45
0x3469	[7:0]	grid_R_Gain_3_2	RW	grid_R_Gain_3_2_addr	-	-	0x61
0x346A	[7:0]	grid_R_Gain_4_2	RW	grid_R_Gain_4_2_addr	-	-	0x95
0x346B	[7:0]	grid_R_Gain_0_3	RW	grid_R_Gain_0_3_addr	-	-	0x99
0x346C	[7:0]	grid_R_Gain_1_3	RW	grid_R_Gain_1_3_addr	-	-	0x80
0x346D	[7:0]	grid_R_Gain_2_3	RW	grid_R_Gain_2_3_addr	-	-	0x73
0x346E	[7:0]	grid_R_Gain_3_3	RW	grid_R_Gain_3_3_addr	-	-	0x85
0x346F	[7:0]	grid_R_Gain_4_3	RW	grid_R_Gain_4_3_addr	-	-	0x9D

10.22. OSD control parameter registers [0x4400 – 0x4421]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x4400	[7:0]	OSD_CTRL	RW	[7]: 1: Neglect blink attribute in the color palette for overlay layer2. All colors will blink when the L2_BLINK_PERIOD is larger than 0. 0: Reference blink attributes in the color palette [6]: 1: Neglect blink attribute in the color palette for overlay layer1. All colors will blink when the L1_BLINK_PERIOD is larger than 0. 0: Reference blink attributes in the color palette [5]: 1: Neglect alpha attribute in the color palette for overlay layer2. All colors will become opaque **(alpha=7)** 0: Reference alpha attributes in the color palette [4]: 1: Neglect alpha attribute in the color palette for overlay layer1. All colors will become opaque **(alpha=7)** 0: Reference alpha attributes in the color palette [3]: 1: Dynamic layer **(L2)** buffer index **(B2_ADDR)** will be updated automatically by S2_ADDR when SPI controller completes to move an OSD image from external memories to OSD buffers for layer 2 data in AB buffer mode **(abbuf_en =1)** 0: B2_ADDR need to be updated manually [2]: 1: Enable overlay display 0: Disable overlay display [1]: 1: Enable layer2 overlay display when global_overlay_en =1 0: Disable layer2 overlay display [0]: 1: Enable layer1 overlay display when global_overlay_en =1 0: Disable layer1 overlay display	-	-	0x00
0x4401	[4:0]	OSD_ERR	RO	[4]: 1: Overlay data move error flag. Overlay data in internal buffer could be incorrect. Read this flag when OSD data transferring is finished [3:2]: retry_cnt_L2 reports the SPI control re-read counts for layer2 when there are CRC fails. Read this value when OSD data transferring is finished [1:0]: retry_cnt_L1 reports the SPI control re-read counts for layer1 when there are CRC fails. Read this value when OSD data transferring is finished	Y	-	0x00

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x4402	[3:0]	OSD_CTRL2	RW	[3]: 1: Disable overlay display when there are CRC fails [2]: Enable AB buffer mode for dynamic overlay. The internal buffer size should be enough to store two images for the dynamic layer. [1]: 1: Enable layer2 data transferring from external memories to internal memories 0: Disable layer2 data transferring [0]: 1: Enable layer1 data transferring from external memories to internal memories 0: Disable layer1 data transferring	-	-	0x00
0x4403	[0]	OSD_MOVE	RW	Write 1 to trigger an OSD data transferring from external memories to internal buffers if l1_load_en or l2_load_en is enabled	-	-	0x00
0x4404	[0]	OSD_FLAG	RW	When an OSD data transferring is complete, this flag will set to 1 automatically. It should be cleared manually before next OSD data transferring is triggered	-	-	0x00
0x4405	[3:0]	OSD_SCALE_CTRL	RW	[3:2]: Layer2 scale mode **(H: Horizontal, V: Vertical)** 00: Hx1, Vx1 01: Hx2, Vx1 10: Hx1, Vx2 11: Hx2, Vx2 [1:0]: Layer1 scale mode **(H: Horizontal, V: Vertical)** 00: Hx1, Vx1 01: Hx2, Vx1 10: Hx1, Vx2 11: Hx2, Vx2	-	-	0x00
0x4406	[3:0]	OSD_OFFSET_SIGN	RW	[3]: Layer2 vertical display offset **(sign and magnitude)** {L2_Y_OFFSET_SIGN **(0:+/1:-**), L2_Y_OFFSET} [2]: Layer2 horizontal display offset **(sign and magnitude)** {L2_X_OFFSET_SIGN **(0:+/1:-)**, L2_X_OFFSET} [1]: Layer1 vertical display offset **(sign and magnitude)** {L1_Y_OFFSET_SIGN **(0:+/1:-)**, L1_Y_OFFSET} [0]: Layer1 horizontal display offset **(sign and magnitude)** {L1_X_OFFSET_SIGN **(0:+/1:-)**, L1_X_OFFSET}	-	-	0x00
0x4407	[7:0]	OSD_L1_XOFFSET	RW	Layer1 horizontal display offset **(sign and magnitude)** {L1_X_OFFSET_SIGN **(0:+/1:-)**, L1_X_OFFSET}	-	-	0x00
0x4408	[7:0]	OSD_L1_YOFFSET	RW	Layer1 vertical display offset **(sign and magnitude)** {L1_Y_OFFSET_SIGN **(0:+/1:-)**, L1_Y_OFFSET}	-	-	0x00
0x4409	[7:0]	OSD_L2_XOFFSET	RW	Layer2 horizontal display offset **(sign and magnitude)** {L2_X_OFFSET_SIGN **(0:+/1:-)**, L2_X_OFFSET}	-	-	0x00

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x440A	[7:0]	OSD_L2_YOFFSET	RW	Layer2 vertical display offset **(sign and magnitude)** {L2_Y_OFFSET_SIGN **(0:+/1:-)**, L2_Y_OFFSET}	-	-	0x00
0x440B	[7:0]	OSD_L1_BLINK	RW	Layer1 blink period. Overlay will switch on and off every L1_BLINK_PERIODx10 frames. Set 0 to disable blinking function.	-	-	0x00
0x440C	[7:0]	OSD_L1_BLINK	RW	Layer2 blink period. Overlay will switch on and off every L2_BLINK_PERIODx10 frames. Set 0 to disable blinking function.	-	-	0x00
0x440D	[3:0]	OSD_TIMEOUT_H	RW	[3:2] Layer2 overlay will switch off after {L2_TIMEOUT_H, L2_TIMEOUT_L} x 10 frames. Set 0 to disable timeout function. [1:0] Layer1 overlay will switch off after {L1_TIMEOUT_H, L1_TIMEOUT_L} x 10 frames. Set 0 to disable timeout function.	-	-	0x00
0x440E	[7:0]	OSD_L1_TIMEOUT_L	RW	Layer1 overlay will switch off after {L1_TIMEOUT_H, L1_TIMEOUT_L} x 10 frames. Set 0 to disable timeout function.	-	-	0x00
0x440F	[7:0]	OSD_L2_TIMEOUT_L	RW	Layer2 overlay will switch off after {L2_TIMEOUT_H, L2_TIMEOUT_L} x 10 frames. Set 0 to disable timeout function.	-	-	0x00
0x4410	[7:0]	OSD_BUF_ADDR_H	RW	[7:4]: Start address in the internal buffer for overlay layer2 data. **(in the unit of 2 bytes)** {B2_ADDR_H, B2_ADDR_L}, default value is 0x800 [3:0]: Start address in the internal buffer for overlay layer1 data. **(in the unit of 2 bytes)** {B1_ADDR_H, B1_ADDR_L}, default value is 0x000	-	-	0x80
0x4411	[7:0]	OSD_L1_BUF_ADDR_L	RW	Start address in the internal buffer for overlay layer1 data. **(in the unit of 2 bytes)** {B1_ADDR_H, B1_ADDR_L}, default value is 0x000	-	-	0x00
0x4412	[7:0]	OSD_L2_BUF_ADDR_L	RW	Start address in the internal buffer for overlay layer2 data. **(in the unit of 2 bytes)** {B2_ADDR_H, B2_ADDR_L}, default value is 0x800	-	-	0x00
0x4417	[7:0]	OSD_DEST_ADDR_H	RW	[7:4]: Destination address for layer2 OSD data transferring from external memories to internal buffers. **(in the unit of 2bytes)** {S2_ADDR_H, S2_ADDR_L}, default value is 0x800 [3:0]: Destination address for layer1 OSD data transferring from external memories to internal buffers. **(in the unit of 2bytes)** {S1_ADDR_H, S1_ADDR_L}, default value is 0x000	-	-	0x80

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x4418	[7:0]	OSD_L1_DEST_ADDR_L	RW	Destination address for layer1 OSD data transferring from external memories to internal buffers. **(in the unit of 2bytes)** {S1_ADDR_H, S1_ADDR_L}, default value is 0x000	-	-	0x00
0x4419	[7:0]	OSD_L2_DEST_ADDR_L	RW	Destination address for layer2 OSD data transferring from external memories to internal buffers. **(in the unit of 2bytes)** {S2_ADDR_H, S2_ADDR_L}, default value is 0x800	-	-	0x00
0x441A	[5:0]	OSD_L1_SIZE_H	RW	Layer1 size for OSD data transferring from external memories to internal buffers. **(in the unit of 1byte)** {S1_SIZE_H, S1_SIZE_L}, default value is 0x1000, range is 14'd0~14'd8192	-	-	0x10
0x441B	[7:0]	OSD_L1_SIZE_L	RW	Reserved	-	-	0x00
0x441C	[5:0]	OSD_L2_SIZE_H	RW	Layer2 size for OSD data transferring from external memories to internal buffers. **(in the unit of 1byte)** {S2_SIZE_H, S2_SIZE_L}, default value is 0x1000, range is 14'd0~14'd8192	-	-	0x10
0x441D	[7:0]	OSD_L2_SIZE_L	RW	Reserved	-	-	0x00
0x441E	[3:0]	OSD_SRC_ADDR_H	RW	[3:2]: Source address for layer2 OSD data transferring from external memories to internal buffers. **(in the unit of 1K bytes)** {L2_ADDR_H, L2_ADDR_L}, default value is 0x004 [1:0]: Source address for layer1 OSD data transferring from external memories to internal buffers. **(in the unit of 1K bytes)** {L1_ADDR_H, L1_ADDR_L}, default value is 0x000	-	-	0x00
0x441F	[7:0]	OSD_L1_SRC_ADDR_L	RW	Source address for layer1 OSD data transferring from external memories to internal buffers. **(in the unit of 1K bytes)** {L1_ADDR_H, L1_ADDR_L}, default value is 0x000	-	-	0x00
0x4420	[7:0]	OSD_L2_SRC_ADDR_L	RW	Source address for layer2 OSD data transferring from external memories to internal buffers. **(in the unit of 1K bytes)** {L2_ADDR_H, L2_ADDR_L}, default value is 0x004	-	-	0x04
0x4421	[0]	OSD_CMU	RW	Write this register to activate OFFSET and B1_ADDR registers simultaneously.	-	-	0x00

10.23. BLC control parameter registers [0x5010]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x5010	[7:0]	BLCTGT	RW	BLC target	Y	-	0x20

10.24. Temperature sensor registers [0x5040 – 0x504A]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x5040	[1:0]	TS_EN	RW	[1]: Temp auto mode enable 0: When Streaming or Stop mode, set to 0 for SINGLE TRIGGER mode 1: When Streaming mode, set to 1 for CONTINUOUS TRIGGER mode [0]: Temp enable	-	-	0x00
0x5045	[0]	TS_TRIGGER	WO	[0]: Set to 1 to trigger for Single Trigger mode **(Streaming and Stop Mode only)**	-	Y	0xFF
0x5046	[0]	TS_VALID	RO	[0]: Temp value ready indicator	Y	-	-
0x5047	[6:0]	TS_VALUE	RO	[6:0]: Temp value read back register TEMP**(C°)**= -45 + 1.5625 **(C°/DN)** * TS_VALUE	Y	-	-
0x504A	[2:0]	TS_MODE	RW	[2]: TS_AUTO_EN [1:0]: Reserved	-	-	0x00

10.25. Analog Registers [0x5229 – 0x522B]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x5229	[7:0]	IOPADTOP1	RW	[7:5]: sr_d [4:2]: s_d [1]: mclk_pd_d [0]: xtal_pd_d	-	-	0x00
0x522A	[7:0]	IOPADTOP2	RW	[7:6]: Reserved [5:3]: sr_pclko_d [2:0]: s_pclko_d	-	-	0x00
0x522B	[7:0]	IOPADTOP3	RW	[7:6]: Reserved [5:3]: sr_spi_d [2:0]: s_spi_d	-	-	0x00

10.26. Synchronization registers [0x5290 – 0x529E]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x5290	[1]	EXPO_SYNC_CONFIG	RW	[1]: Read Synchronization enable	-	-	0x00
0x5293	[0]	Error_flag_config	RW	[0]: Error Flag self clear enable	-	-	0x01
0x5296	[3:0]	TD_readsync_MSB	RO	Delay between Master sensor and Slave sensor in Read Synchronization mode	-	-	-
0x5297	[7:0]	TD_readsync_H	RO	Delay between Master sensor and Slave sensor in Read Synchronization mode	-	-	-
0x5298	[7:0]	TD_readsync_L	RO	Delay between Master sensor and Slave sensor in Read Synchronization mode	-	-	-
0x5299	[7:0]	Offset_readsync_H	RW	Adjustment Register for TD in Read Synchronization mode **(Scale: one half row)** [7]: Signed bit	-	-	0x00
0x529A	[7:0]	Offset_readsync_L	RW	Adjustment Register for TD in Read Synchronization mode **(Scale: one half row)**	-	-	0x00
0x529B	[7:0]	Readsync_decodethreshold_H	RW	Threshold for Out-of-Sync in Read Synchronization mode **(Scale: one half row)**	-	-	0x20
0x529C	[7:0]	Readsync_decodethreshold_L	RW	Threshold for Out-of-Sync in Read Synchronization mode **(Scale: one half row)**	-	-	0x80
0x529E	[7:0]	Readsync_error_flag	RO	Out-of-sync indicator in Read Synchronization mode	-	-	-

10.27. LED IRS registers [0x5400 – 0x5405]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x5400	[7:0]	LEDIRS_CTRL	RW	[7:6]: Reserved. [5]: IRS0, IRS1 output polarity control 1: negative, 0: positive. [4]: LED output polarity control 1: negative, 0: positive. [3]: IRSI input polarity control. 1: negative, 0: positive. [2]: BW_LED enable. [1]: IRS enable. **(when [0], [1], IRS0 & IRS1 is output)** [0]: LED output enable. **(when [0], [1] enabled, IRLED is output)**	-	-	0x07
0x5401	[7:0]	LED_HY_PERIOD	RW	Hysteresis period for IRSI signal to stable. **(unit: DivTime)**	-	-	0xC0
0x5402	[7:0]	IRS_PERIOD	RW	IR switch on period. **(unit: DivTime)**	-	-	0x20
0x5403	[7:0]	DIV_CTRL	RW	[7:1]: Reserved. [0]: Divide control enable.	-	-	0x01
0x5404	[7:0]	DIV_CNT	RW	DivTime = (2* DIV_CNT) * RefTime.	-	-	0xA0
0x5405	[7:0]	RefTimerCNT	RW	RefTime = (2* RefTimerCNT) * Tclk_period.	-	-	0x77

10.28. Functional safety registers [0x7000 – 0x700A]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x7000	[5:0]	SAFETY_FLAG	RO	All flags are cleared when 0x7000 is read. [5]: TEMP_ERR_FLAG is set when the operating temperature is out of range. [4]: AVDD_BO_FLAG is set when AVDD brown-out event happens. [3]: SRAM_BIST_ERR_FLAG is set when SRAM BIST done during power up returns error. [2]:TEST_PTRN_ERR_FLAG is set when auto self-test during boot sequence returns CRC error. [1]: SPI_CRC_ERR_FLAG is set when loading boot data from external SPI device returns CRC error. [0]: I2C_CRC_ERR_FLAG is set when loading boot data from external I2C device returns CRC error.	Y	-	0x00
0x7001	[5:0]	SAFETY_PO_EN	RW	[5]: TEMP_OOR_PO_EN Set if a flag triggers brown-out pin indicator assertion is desired. [4]: AVDD_BO_PO_EN [3]: SRAM_BIST_PO_EN [2]: TEST_PTRN_PO_EN [1]: SPI_ERR_PO_EN [0]: I2C_ERR_PO_EN	-	-	0x00
0x7003	[1:0]	SRAM_BIST_STATUS	RO	[1]: BIST_FAIL [0]: BIST_DONE After SRAM BIST is finished, {BIST_FAIL, BIST_DONE} is 2'b01 if test is OK and 2'b11 if test fails. After 0x7000 is read {BIST_FAIL, BIST_DONE} is cleared to 2'b10.	-	-	0x02
0x7004	[7:0]	TEST_PTRN_CRC_H	RW	TEST_PTRN_CRC[15:0] is used to compare with internally calculated test pattern CRC value. [7:0]:TEST_PTRN_CRC[15:8]	Y	-	0x00
0x7005	[7:0]	TEST_PTRN_CRC_L	RW	[7:0]:TEST_PTRN_CRC[7:0]	Y	-	0x00
0x7006	[6:0]	MAX_TEMP	RW	[6:0]: MAX_TEMP is the maximum operating temperature.	-	-	0x7F
0x7007	[6:0]	MIN_TEMP	RW	[6:0]: MIN_TEMP is the minimum operating temperature.	-	-	0x00
0x7008	[3:0]	SAFETY_CTRL	RW	[3]: TEMP_ERR_ARM needs to be set after the temperature out-of-range is detected. **(W/O)** [2]: AVDD_BO_ARM needs to be set after AVDD brown-out is detected. **(W/O)** [1]: AVDD_BO_ZERO_OUT: of set, output port will stream out 0's when AVDD brown-out happens. [0]: TEMP_ERR_ZERO_OUT: if set, output port will stream out 0's when temperature out-of-range happens.	-	-	0x00

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0x7009	[7:0]	IMAGE_CHKSUM_HB	RW	IMAGE_CHKSUM stores the calculated CRC-16 checksum of the latest image. [7:0]: IMAGE_CHKSUM[15:8]	Y	-	-
0x700A	[7:0]	IMAGE_CHKSUM_LB	RW	[7:0]: IMAGE_CHKSUM[7:0]	Y	-	-

10.29. YUV_ISP control & parameter registers [0xD120 – 0XD126]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD120	[6:0]	ISP_CTRL1	RW	ISP function control byte1 [6]: Reserved [5]: AE weight mode enable 0: OFF **1: ON** [4]: Hue control bit 0: OFF **1: ON** [3]: Reserved [2]: Gamma control 0: OFF **1: ON** [1]: Reserved [0]: Anti-flicker reference frequency 0: 50Hz **1: 60Hz**	-	Y	0x37
0xD121	[7:0]	ISP_CTRL2	RW	ISP function control byte2 [7:6]: Reserved [5]: Hue-Sin signal bit **0: plus** 1: minus [4]: Hue-Cos signal bit **0: plus** 1: minus [3:2]: Reserved [1]: AE DRO mode DRO Enable **0: OFF** 1: ON [0]: Reserved	-	Y	0x81
0xD124	[7:3]	CCM_CTRL1	RW	CCM_Ctrl_Byte [7]: CT1_coef_sign [6]: CT0_coef_sign [5]: CCM_BYPASS [4]: CCM_ON [3]: Reserved	-		0xDE
0xD125	[7:0]	YUV_CTRL1	RW	[7]: Contrast function 0: OFF **1: ON** [6]: Brightness function 0: OFF **1: ON** [5]: Scaling function **0: OFF** 1: ON [4]: Windowing function 0: OFF **1: ON** [3]: Y denoise function 0: OFF **1: ON** [2]: Reserved [1]: Y Sharpness function 0: OFF **1: ON** [0]: Fade to black **(F2B)** function 0: OFF **1: ON**	-	Y	0xDF
0xD126	[7:0]	YUV_CTRL2	RW	[7]: NA [6:1]: Reserved [0]: Y-directional denoise Enable Y Denoise2 0: OFF 1: ON	-	Y	0x6D

10.30. Gamma control & parameter registers [0XD280 – 0XD307]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD280	[7:0]	GAMMA1_L	RW	GAMMA1 y axis **(Low Byte)**	-	Y	0x0D
0xD281	[1:0]	GAMMA1_H	WO	GAMMA1 y axis **(High Byte)**	-	Y	-
0xD282	[7:0]	GAMMA2_L	RW	GAMMA2 y axis **(Low Byte)**	-	Y	0x1A
0xD283	[1:0]	GAMMA2_H	WO	GAMMA2 y axis **(High Byte)**	-	Y	-
0xD284	[7:0]	GAMMA3_L	RW	GAMMA3 y axis **(Low Byte)**	-	Y	0x30
0xD285	[1:0]	GAMMA3_H	WO	GAMMA3 y axis **(High Byte)**	-	Y	-
0xD286	[7:0]	GAMMA4_L	RW	GAMMA4 y axis **(Low Byte)**	-	Y	0x53
0xD287	[1:0]	GAMMA4_H	WO	GAMMA4 y axis **(High Byte)**	-	Y	-
0xD288	[7:0]	GAMMA5_L	RW	GAMMA5 y axis **(Low Byte)**	-	Y	0x62
0xD289	[1:0]	GAMMA5_H	WO	GAMMA5 y axis **(High Byte)**	-	Y	-
0xD28A	[7:0]	GAMMA6_L	RW	GAMMA6 y axis **(Low Byte)**	-	Y	0x6E
0xD28B	[1:0]	GAMMA6_H	WO	GAMMA6 y axis **(High Byte)**	-	Y	-
0xD28C	[7:0]	GAMMA7_L	RW	GAMMA7 y axis **(Low Byte)**	-	Y	0x7A
0xD28D	[1:0]	GAMMA7_H	WO	GAMMA7 y axis **(High Byte)**	-	Y	-
0xD28E	[7:0]	GAMMA8_L	RW	GAMMA8 y axis (**Low Byte)**	-	Y	0x83
0xD28F	[1:0]	GAMMA8_H	WO	GAMMA8 y axis **(High Byte)**	-	Y	-
0xD290	[7:0]	GAMMA9_L	RW	GAMMA9 y axis **(Low Byte)**	-	Y	0x8B
0xD291	[1:0]	GAMMA9_H	WO	GAMMA9 y axis **(High Byte)**	-	Y	-
0xD292	[7:0]	GAMMA10_L	RW	GAMMA10 y axis **(Low Byte)**	-	Y	0x92
0xD293	[1:0]	GAMMA10_H	WO	GAMMA10 y axis **(High Byte)**	-	Y	-
0xD294	[7:0]	GAMMA11_L	RW	GAMMA11 y axis **(Low Byte)**	-	Y	0x9D
0xD295	[1:0]	GAMMA11_H	WO	GAMMA11 y axis **(High Byte)**	-	Y	-
0xD296	[7:0]	GAMMA12_L	RW	GAMMA12 y axis **(Low Byte)**	-	Y	0xA8
0xD297	[1:0]	GAMMA12_H	WO	GAMMA12 y axis **(High Byte)**	-	Y	-
0xD298	[7:0]	GAMMA13_L	RW	GAMMA13 y axis **(Low Byte)**	-	Y	0xBC
0xD299	[1:0]	GAMMA13_H	WO	GAMMA13 y axis **(High Byte)**	-	Y	-
0xD29A	[7:0]	GAMMA14_L	RW	GAMMA14 y axis **(Low Byte)**	-	Y	0xCF
0xD29B	[1:0]	GAMMA14_H	WO	GAMMA14 y axis **(High Byte)**	-	Y	-
0xD29C	[7:0]	GAMMA15_L	RW	GAMMA15 y axis **(Low Byte)**	-	Y	0xE2
0xD29D	[1:0]	GAMMA15_H	WO	GAMMA15 y axis **(High Byte)**	-	Y	-
0xD29E	[7:0]	GAMMASLOPE_L	RW	GAMMASLOP **(Low Byte)**	-	Y	0x2A
0xD29F	[1:0]	GAMMASLOPE_H	WO	GAMMASLOP **(High Byte)**	-	Y	-
0xD2A0	[3:0]	GAMMA_LL	RW	GAMMA_ALPHA	-	Y	0x02
0xD2C0	[7:0]	CCM00_L	RW	NormCCM00_LB[7:0]	-	-	0x7D
0xD2C1	[1:0]	CCM00_H	RW	NormCCM00_HB[1:0]	-	-	0x01
0xD2C2	[7:0]	CCM01_L	RW	NormCCM01_LB[7:0]	-	-	0x84
0xD2C3	[2:0]	CCM01_H	RW	NormCCM01_HB[2:0]	-	-	0x07
0xD2C4	[7:0]	CCM02_L	RW	NormCCM02_LB[7:0]	-	-	0xFF
0xD2C5	[2:0]	CCM02_H	RW	NormCCM02_HB[2:0]	-	-	0x07
0xD2C6	[7:0]	CCM10_L	RW	NormCCM10_LB[7:0]	-	-	0xC2
0xD2C7	[2:0]	CCM10_H	RW	NormCCM10_HB[2:0]	-	-	0x07
0xD2C8	[7:0]	CCM11_L	RW	NormCCM11_LB[7:0]	-	-	0x90
0xD2C9	[1:0]	CCM11_H	RW	NormCCM11_HB[1:0]	-	-	0x01
0xD2CA	[7:0]	CCM12_L	RW	NormCCM12_LB[7:0]	-	-	0xAE
0xD2CB	[2:0]	CCM12_H	RW	NormCCM12_HB[2:0]	-	-	0x07
0xD2CC	[7:0]	CCM20_L	RW	NormCCM20_LB[7:0]	-	-	0xFC
0xD2CD	[2:0]	CCM20_H	RW	NormCCM20_HB[2:0]	-	-	0x07
0xD2CE	[7:0]	CCM21_L	RW	NormCCM21_LB[7:0]	-	-	0x57
0xD2CF	[2:0]	CCM21_H	RW	NormCCM21_HB[2:0]	-	-	0x07
0xD2D0	[7:0]	CCM22_L	RW	NormCCM22_LB[7:0]	-	-	0xAD
0xD2D1	[1:0]	CCM22_H	RW	NormCCM22_HB[1:0]	-	-	0x01
0xD2E0	[3:0]	CCM_LL	RW	CCM_ALPHA[3:0]	-	-	0x04
0xD2F0	[7:0]	ACCM00_L	RW	ACCM00_LB[7:0]	-	-	0xB2
0xD2F1	[2:0]	ACCM00_H	RW	ACCM00_HB[2:0]	-	-	0x07
0xD2F2	[7:0]	ACCM01_L	RW	ACCM01_LB[7:0]	-	-	0xB1
0xD2F3	[2:0]	ACCM01_H	RW	ACCM01_HB[2:0]	-	-	0x00
0xD2F4	[7:0]	ACCM02_L	RW	ACCM02_LB[7:0]	-	-	0x9D
0xD2F5	[2:0]	ACCM02_H	RW	ACCM02_HB[2:0]	-	-	0x07
0xD2F6	[7:0]	ACCM10_L	RW	ACCM10_LB[7:0]	-	-	0xD8
0xD2F7	[2:0]	ACCM10_H	RW	ACCM10_HB[2:0]	-	-	0x07

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD2F8	[7:0]	ACCM11_L	RW	ACCM11_LB[7:0]	-	-	0xD7
0xD2F9	[2:0]	ACCM11_H	RW	ACCM11_HB[2:0]	-	-	0x07
0xD2FA	[7:0]	ACCM12_L	RW	ACCM12_LB[7:0]	-	-	0x51
0xD2FB	[2:0]	ACCM12_H	RW	ACCM12_HB[2:0]	-	-	0x00
0xD2FC	[7:0]	ACCM20_L	RW	ACCM20_LB[7:0]	-	-	0x9C
0xD2FD	[2:0]	ACCM20_H	RW	ACCM20_HB[2:0]	-	-	0x07
0xD2FE	[7:0]	ACCM21_L	RW	ACCM21_LB[7:0]	-	-	0x95
0xD2FF	[2:0]	ACCM21_H	RW	ACCM21_HB[2:0]	-	-	0x07
0xD300	[7:0]	ACCM22_L	RW	ACCM22_LB[7:0]	-	-	0xCF
0xD301	[2:0]	ACCM22_H	RW	ACCM22_HB[2:0]	-	-	0x00
0xD302	[6:0]	CCM03	RW	NormCCM03[6:0]	-	-	0x00
0xD303	[6:0]	CCM13	RW	NormCCM13[6:0]	-	-	0x00
0xD304	[6:0]	CCM23	RW	NormCCM23[6:0]	-	-	0x00
0xD305	[6:0]	ACCM03	RW	ACCM03[6:0]	-	-	0x00
0xD306	[6:0]	ACCM13	RW	ACCM13[6:0]	-	-	0x00
0xD307	[6:0]	ACCM23	RW	ACCM23[6:0]	-	-	0x00

10.31. BLI parameter registers [0XD308]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD308	[7:0]	BLI_TGT	RW	BLI_TARGET[7:0]	-	Y	0x00

10.32. AE registers [0xD380 – 0xD3F2]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD380	[1:0]	AEAWBCFG	RW	AE and AWB Control [1]: AWB enable 0: bypass 1: ON [0]: AE enable 0: bypass 1: ON	-	Y	0xFF
0xD381	[7:0]	AETARGU	RW	[7:0]: AE target mean upper bound setting	-	-	0x48
0xD382	[7:0]	AETARGL	RW	[7:0]: AE target mean lower bound setting	-	-	0x30
0xD38A	[7:0]	AETDAMP	RW	[7:0]: AE setting of T-Damping	-	-	0x80
0xD38B	[7:0]	AENDAMP	RW	[7:0]: AE setting of N-Damping	-	-	0x0A
0xD38E	[7:0]	AETARGM	RW	[7:0]: AE target mean value	-	Y	0X3C
0xD38F	[7:0]	AEMXEXH	RW	[7:0]: AE maximum exposure setting high byte **(MSB)**	-	-	0X02
0xD390	[7:0]	AEMXEXL	RW	[7:0]: AE maximum exposure setting low byte **(LSB)**	-	-	0X34
0xD391	[7:0]	AEMNEX	RW	[7:0]: AE minimum exposure setting	-	-	0X01
0xD392	[7:0]	AEMXAG	RW	[7:0]: AE setting of maximum coarse analog gain	-	-	0X03
0xD393	[7:0]	AEMXDG	RW	[7:0]: AE setting of maximum digital gain and fine analog gain	-	-	0X80
0xD394	[7:0]	AEMNDG	RW	[7:0]: AE setting of minimum digital gain	-	-	0X40
0xD395	[7:0]	AESKIP	RW	AE setting of PG-FM skip count [7:4]: AWB_pg_skipcnt [3:0]: AE_pg_skipcnt	-	-	0X23
0xD3B3	[7:0]	AE_WIN_ORG_V_L	RW	[7:0]: AE 5x5 window vertical origin **(low byte)**	-	-	0X10
0xD3B4	[7:0]	AE_WIN_ORG_V_H	RW	[7:0]: AE 5x5 window vertical origin **(high byte)**	-	-	0X00
0xD3B5	[7:0]	AE_WIN_ORG_H_L	RW	[7:0]: AE 5x5 window horizontal origin **(low byte)**	-	-	0X10
0xD3B6	[7:0]	AE_WIN_ORG_H_H	RW	[7:0]: AE 5x5 window horizontal origin **(high byte)**	-	-	0X00
0xD3B7	[7:0]	AE_WIN_STEP_V_L	RW	[7:0]: AE 5x5 window vertical step **(low byte)**	-	-	0XA0
0xD3B8	[7:0]	AE_WIN_STEP_V_H	RW	[7:0]: AE 5x5 window vertical step **(high byte)**	-	-	0X00
0xD3B9	[7:0]	AE_WIN_STEP_H_L	RW	[7:0]: AE 5x5 window horizontal step **(low byte)**	-	-	0XC8
0xD3BA	[7:0]	AE_WIN_STEP_H_H	RW	[7:0]: AE 5x5 window horizontal step **(high byte)**	-	-	0X00
0xD3C2	[7:0]	AE_AVG_BV	RO	Reserved	Y	-	-
0xD3E0	[6:4] [2:0]	AE_WIN_WT_1_12	RW	Window weight **000: 0%,** **001: 12.5%,** **010: 25.0%,** **011: 50.0%,** **100: 75.0%,** **101: 87.5%,** **110: 100%** [6:4]: WinWeight_1_2 [2:0]: WinWeight_1_1	-	-	0x10
0xD3E1	[6:4] [2:0]	AE_WIN_WT_1_34	RW	[6:4]: WinWeight_1_4 [2:0]: WinWeight_1_3	-	-	0X01
0xD3E2	[2:0]	AE_WIN_WT_1_56	RW	[2:0]: WinWeight_1_5	-	-	0X04

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD3E4	[6:4] [2:0]	AE_WIN_WT_2_12	RW	[6:4]: WinWeight_2_2 [2:0]: WinWeight_2_1	-	-	0X21
0xD3E5	[6:4] [2:0]	AE_WIN_WT_2_34	RW	[6:4]: WinWeight_2_4 [2:0]: WinWeight_2_3	-	-	0X12
0xD3E6	[2:0]	AE_WIN_WT_2_56	RW	[2:0]: WinWeight_2_5	-	-	0X04
0xD3E8	[6:4] [2:0]	AE_WIN_WT_3_12	RW	[6:4]: WinWeight_3_2 [2:0]: WinWeight_3_1	-	-	0X32
0xD3E9	[6:4] [2:0]	AE_WIN_WT_3_34	RW	[6:4]: WinWeight_3_4 [2:0]: WinWeight_3_3	-	-	0X23
0xD3EA	[2:0]	AE_WIN_WT_3_56	RW	[2:0]: WinWeight_3_5	-	-	0X04
0xD3EC	[6:4] [2:0]	AE_WIN_WT_4_12	RW	[6:4]: WinWeight_4_2 [2:0]: WinWeight_4_1	-	-	0X21
0xD3ED	[6:4] [2:0]	AE_WIN_WT_4_34	RW	[6:4]: WinWeight_4_4 [2:0]: WinWeight_4_3	-	-	0X12
0xD3EE	[2:0]	AE_WIN_WT_4_56	RW	[2:0]: WinWeight_4_5	-	-	0X04
0xD3F0	[6:4] [2:0]	AE_WIN_WT_5_12	RW	[6:4]: WinWeight_5_2 [2:0]: WinWeight_5_1	-	-	0X44
0xD3F1	[6:4] [2:0]	AE_WIN_WT_5_34	RW	[6:4]: WinWeight_5_4 [2:0]: WinWeight_5_3	-	-	0X44
0xD3F2	[2:0]	AE_WIN_WT_6_56	RW	[2:0]: WinWeight_5_5	-	-	0X04

10.33. Contrast control & parameter registers [0xD490 – 0xD4AF]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD490	[7:0]	CONTRAST_X1	RW	Contrast_X1	-	-	0x10
0xD492	[7:0]	Contrast_X2	RW	Contrast_X2	-	-	0x30
0xD494	[7:0]	Contrast_X3	RW	Contrast_X3	-	-	0x70
0xD496	[7:0]	Contrast_X4	RW	Contrast_X4	-	-	0x90
0xD498	[7:0]	Contrast_X5	RW	Contrast_X5	-	-	0xD0
0xD49A	[7:0]	Contrast_X6	RW	Contrast_X6	-	-	0xF0
0xD49C	[7:0]	Contrast_P0_LL	RW	Contrast_P0_alpha	-	-	0x00
0xD49D	[7:0]	Contrast_P1	RW	Contrast_P1	-	-	0x10
0xD49E	[7:0]	Contrast_P1_LL	RW	Contrast_P1_alpha	-	-	0x10
0xD4A0	[7:0]	Contrast_P2	RW	Contrast_P2	-	-	0x30
0xD4A3	[7:0]	Contrast_P3	RW	Contrast_P3	-	-	0x70
0xD4A4	[7:0]	Contrast_P3_LL	RW	Contrast_P3_alpha	-	-	0x70
0xD4A6	[7:0]	Contrast_P4	RW	Contrast_P4	-	-	0x90
0xD4A7	[7:0]	Contrast_P4_LL	RW	Contrast_P4_alpha	-	-	0x90
0xD4A9	[7:0]	Contrast_P5	RW	Contrast_P5	-	-	0xD0
0xD4AA	[7:0]	Contrast_P5_LL	RW	Contrast_P5_alpha	-	-	0xD0
0xD4AC	[7:0]	Contrast_P6	RW	Contrast_P6	-	-	0xF0
0xD4AD	[7:0]	Contrast_P6_LL	RW	Contrast_P6_alpha	-	-	0xF0
0xD4AF	[7:0]	Contrast_P7_LL	RW	Contrast_P7_alpha	-	-	0xFF

10.34. Brightness control & parameter registers [0xD4C0 – 0xD4C1]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD4C0	[7:0]	BRIGHT_CTRL	RW	[7]: Brightness sign [6:0]: Brightness level	-	-	0x00
0xD4C1	[7:0]	BRIGHT_LL	RW	[7]: Brightness sing alpha [6:0]: Brightness level alpha	-	-	0x00

10.35. Flicker control & parameter registers [0xD540 – 0xD54F]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD540	[7:0]	FLK_STP_60_H	RW	AE flicker step 60Hz **(high byte)**	-	-	0x00
0xD541	[7:0]	FLK_STP_60_L	RW	AE flicker step 60Hz **(low byte)**	-	-	0x4F
0xD542	[7:0]	FLK_STP_50_H	RW	AE flicker step 50Hz **(high byte)**	-	-	0x00
0xD543	[7:0]	FLK_STP_50_L	RW	AE flicker step 50Hz **(low byte)**	-	-	0xA9
0xD54F	[7:0]	Flicker Hysteresis	RW	The hyst value to control how long should EGP keep at 1 flicker step. Range: 0~128 (hyst = Flicker_Hyst_TH / 128.0)	-	-	0x80

10.36. Brightness control & parameter registers [0xD5D0 – 0xD5D1]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD5D0	[6:0]	F2B_START	RW	F2B_StartMean	-	-	0x10
0xD5D1	[2:0]	F2B_RANGE	RW	F2B_Range	-	-	0x05

10.37. Digital window control & parameter registers [0xD5E4 – 0xD5EB]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD5E4	[2:0]	DWIN_XOFFSET_H	RW	DWIN_XOFFSET_HB	-	-	0x00
0xD5E5	[7:0]	DWIN_XOFFSET_L	RW	DWIN_XOFFSET_LB	-	-	0x08
0xD5E6	[2:0]	DWIN_XSIZE_H	RW	DWIN_XSIZE_HB	-	-	0x05
0xD5E7	[7:0]	DWIN_XSIZE_L	RW	DWIN_XSIZE_LB	-	-	0x00
0xD5E8	[1:0]	DWIN_YOFFSET_H	RW	DWIN_YOFFSET_HB	-	-	0x00
0xD5E9	[7:0]	DWIN_YOFFSET_L	RW	DWIN_YOFFSET_LB	-	-	0x08
0xD5EA	[1:0]	DWIN_YSIZE_H	RW	DWIN_YSIZE_HB	-	-	0x03
0xD5EB	[7:0]	DWIN_YSIZE_L	RW	DWIN_YSIZE_LB	-	-	0xC0

10.38. Scaler control & parameter registers [0xD5F0 – 0xD5F8]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD5F0	[1:0]	SCAL_HSF_H	RW	Scaler_HSF_HB	-	-	0x02
0xD5F1	[7:0]	SCAL_HSF_L	RW	Scaler_HSF_LB	-	-	0x00
0xD5F2	[1:0]	SCAL_VSF_H	RW	Scaler_VSF_HB	-	-	0x02
0xD5F3	[7:0]	SCAL_VSF_L	RW	Scaler_VSF_LB	-	-	0x00
0xD5F4	[7:0]	DSC_Ctrl_byte1	RW	[7:6]: Down_Scaler_V_Offset [5:4]: Down_Scaler_H_Offset [3]: Reserved [2]: Down_Scaler_resync_opt 0: Free run and re-sync by dsc_resync_on 1: Auto-sync by each frame [1]: Down_Scaler_CLKO_En [0]: Down_Scaler_En	-	-	0x02
0xD5F5	[7:0]	Down_Scaler_HSF_H	RW	Horizontal scaling factor**(HB)**, in/out	-	-	0x50
0xD5F6	[7:0]	Down_Scaler_HSF_L	RW	Horizontal scaling factor**(LB)**, in/out	-	-	0x00
0xD5F7	[7:0]	Down_Scaler_VSF_H	RW	Vertical scaling factor**(HB)**, in/out	-	-	0x50
0xD5F8	[7:0]	Down_Scaler_VSF_L	RW	Vertical scaling factor**(LB)**, in/out	-	-	0x00

10.39. Y denoise 1 parameter registers [0xD709 – 0xD70B]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD709	[4:0]	YDN1_STR	RW	Luma Denoise 1 strength	-	-	0x00
0xD70A	[4:0]	YDN1_STR_LL	RW	Luma Denoise strength_alpha	-	-	0x00
0xD70B	[4:0]	YDN1_STR_UL	RW	Luma Denoise strength_alpha_UL	-	-	0x00

10.40. Y denoise 2 parameter registers [0xD716 – 0xD71E]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD716	[7:0]	YDN2_Y1_TH	RW	Y1 denoise threshold	-	-	0x00
0xD717	[7:0]	YDN2_Y1_TH_LL	RW	Y1 denoise threshold_alpha	-	-	0x00
0xD718	[7:0]	YDN2_Y1_TH_UL	RW	Y1 denoise threshold_alpha_UL	-	-	0x00
0xD719	[7:0]	YDN2_Y2_TH	RW	Y2 denoise threshold	-	-	0x00
0xD71A	[7:0]	YDN2_Y2_TH_LL	RW	Y2 denoise threshold_alpha	-	-	0x00
0xD71B	[7:0]	YDN2_Y2_TH_UL	RW	Y2 denoise threshold _alpha_UL	-	-	0x00
0xD71C	[7:0]	YDN2_Y3_TH	RW	Y3 denoise threshold	-	-	0x00
0xD71D	[7:0]	YDN2_Y3_TH_LL	RW	Y3 denoise threshold_alpha	-	-	0x00
0xD71E	[7:0]	YDN2_Y3_TH_UL	RW	Y3 denoise threshold_alpha_UL	-	-	0x00

10.41. Y sharpness parameter registers [0xD725 – 0xD72A]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD725	[5:0]	SHARP_MF_STR	RW	Ysharp_medium strength Luma Sharpening medium frequency strength	-	-	0x00
0xD726	[5:0]	SHARP_MF_STR_LL	RW	Ysharp_medium strength_alpha [f2.6]	-	-	0x00
0xD727	[5:0]	SHARP_MF_STR_UL	RW	Ysharp_medium strength_alpha_UL [f2.6]	-	-	0x00
0xD728	[5:0]	SHARP_HF_STR	RW	Ysharp_high strength	-	-	0x00
0xD729	[5:0]	SHARP_HF_STR_LL	RW	Ysharp_high strength_alpha	-	-	0x00
0xD72A	[5:0]	SHARP_HF_STR_UL	RW	Ysharp_high strength_alpha_UL	-	-	0x00

10.42. AFD Parameter Registers [0xD770 – 0xD795]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xD770	[4] [0]	AFD_Ctrl	RW	[4]: AFD_update_en [0]: AFD_en	-	-	0x00
0xD795	[7:0]	AFD_result	RO	[7:1]: Reserved [0] 1: 60Hz 0: 50Hz	-	-	-

10.43. SPI-OSD access buffer (write protected) registers [0xE000 – 0xFFFF]

Address	Byte	Register name	Type	Description	EM	CMU	Default (Hex)
0xE000	[7:0]	SPI_OSD_BUF0	RW	SPI_OSD buffer byte 0	-	-	-
0xE001	[7:0]	SPI_OSD_BUF1	RW	SPI_OSD buffer byte 1	-	-	-
				:			
0xFFFF	[7:0]	SPI_OSD_BUF8191	R/W	SPI_OSD buffer byte 8191	-	-	-

Note: (1) When overlay function is enabled, these registers should not be accessed.

11. Electrical Specification

11.1. Absolute maximum ratings

Parameter		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
Ambient storage temperature		T_{ST}	-40	-	125	°C
Operating temperature		T_{OP}	-40	-	105	°C
Stable image temperature(1)		T_{SI}	0	-	70	°C
Analog supply voltage		V_{DD-A_MAX}	-0.3	-	4.0	V
Digital supply voltage		V_{DD-D_MAX}	-0.3	-	2.0	V
IO supply voltage		V_{DD-IO_MAX}	-0.3	-	4.0	V
DC input voltage		DC_{IN}	-0.3	-	V_{DD-IO} + 0.3	V
ESD rating	Human Body Model	ESD	-	2000	-	V
	Machine Model		-	200	-	V

Note: (1) Image side effects outside stable image include pattern noise, and not limited to defect pixels, color and image aberrations, and other conditions. Side effects may reduce progressively upon returning to the stable image temperate range. The image quality is not guaranteed when operating the sensor beyond the stable image temperature specification.

(2) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 11.1: Absolute maximum ratings

11.2. Operating ratings

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Analog supply voltage	V_{DD-A}	3	3.3	3.6	V
Digital supply voltage	V_{DD-D}	1.35	1.5	1.65	V
LDO supply voltage	$V_{DD-LDOIN}$	1.7	1.8	3.6	V
IO supply voltage	V_{DD-IO}	1.7	1.8	3.6	V

Table 11.2: Operating ratings

11.3. DC characteristics

The power consumptions are measured by using internal test pattern. **(Set register 0x0601=0x41)**

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Current Consumption						
Active current	$I_{DD-AVDD}$	Bypass Internal LDO Mode, RAW, full resolution @60FPS, V_{DD-A} = 3.3V, V_{DD-D} = 1.5V, V_{DD-IO} = 3.3V	-	20.2	-	mA
	$I_{DD-DVDD}$		-	66.4	-	
	$I_{DD-IOVDD}$		-	22.3	-	
Active current	$I_{DD-AVDD}$	Internal LDO Mode, RAW, full resolution @60FPS V_{DD-A} = 3.3V, $V_{DD-LDOIN}$ = 3.3V, V_{DD-IO} = 3.3V	-	20.2	-	mA
	$I_{DD-LDOIN}$		-	76.3	-	
	$I_{DD-IOVDD}$		-	22.4	-	
Active current	$I_{DD-AVDD}$	Bypass Internal LDO Mode, YUV, full resolution @30FPS, V_{DD-A} = 3.3V, V_{DD-D} = 1.5V, V_{DD-IO} = 3.3V	-	16.5	-	mA
	$I_{DD-DVDD}$		-	75.9	-	
	$I_{DD-IOVDD}$		-	19.7	-	
Active current	$I_{DD-AVDD}$	Internal LDO Mode, YUV, full resolution @30FPS, V_{DD-A} = 3.3V, $V_{DD-LDOIN}$ = 3.3V, V_{DD-IO} = 3.3V	-	16.5	-	mA
	$I_{DD-LDOIN}$		-	84.3	-	
	$I_{DD-IOVDD}$		-	19.5	-	
Hardware shutdown current	$I_{DD-XSHUTDOWN}$	XSHUTDOWN=0V V_{DD-A} = 3.3V, V_{DD-D} = 3.3V, V_{DD-IO} = 3.3V, MCLK is provided	-	0.5	-	µA
Digital Inputs (MCLK, SCL, XSHUTDOWN)						
Input voltage low	V_{IL}	-	GND - 0.3	-	$0.3V_{DD-IO}$	V
Input voltage high	V_{IH}	-	$0.7V_{DD-IO}$	-	V_{DD-IO} + 0.3	V
Input capacitance	C_{IN}	-	-	4	-	pF
Digital Output						
Output voltage low	V_{OL}	-	-	-	$0.2V_{DD-IO}$	V
Output voltage high	V_{OH}	-	$0.8V_{DD-IO}$	-	-	V
Output capacitance	C_{OUT}	-	-	4	-	pF
Output resistance	R_{OUT}	-	-	1	-	Ω
Tri-state leakage current	I_{OZ}	-	-	-	10	µA

Table 11.3: DC characteristics

11.4. Master clock input

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Input frequency	MCLK	Program PLL Bypass PLL	6	27	27	MHz
Input clock duty cycle	$MCLK_{DUTY}$	-	45	-	55	%

Table 11.4: Master clock (MCLK) timing

11.5. Serial bus characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Input clock frequency	F_{SCL}	-	100	-	1000	kHz
Input clock period	t_{SCL}	-	1	-	10	µs
Input clock duty cycle	-	-	40	50	60	%
Rise time of SCL/SDA	t_{RT}	-	-	-	$0.12T_{SCL}$(1)	ns
Fall time of SCL/SDA	t_{FT}	-	-	-	$0.12T_{SCL}$(1)	ns
Start setup time	t_{HD_SU}	Write	T_{MCLK}(2)	-	-	ns
Start hold time	t_{HD_STA}	Write	$3T_{MCLK}$(2)	-	-	ns
Data hold time	t_{HD_DAT}	Write	5	-	-	ns
Data setup time	t_{SU_DAT}	Write	$3T_{MCLK}$(2)	-	-	ns
Stop setup time	t_{SU_STP}	Write	$3T_{MCLK}$(2)	-	-	ns
Stop hold time	t_{HD_STP}	Write	T_{MCLK}(2)	-	-	ns
Data hold time	t_{HD_DATR}	Read	$3T_{MCLK}$(2)	-	-	ns
Data setup time	t_{SU_DATR}	Read	T_{SCL}(1)/2-t_{HD_DATR}	-	-	ns
SDA maximum load capacitance	C_{SDA_LOAD}	-	-	-	4.2	pF
SDA pull-up resistor	R_{SDA}	-	500	-	-	Ω

Note: (1) T_{SCL} = Cycle time of SCL
(2) T_{MCLK}=Cycle time of MCLK.

Table 11.5: Serial bus interface timing

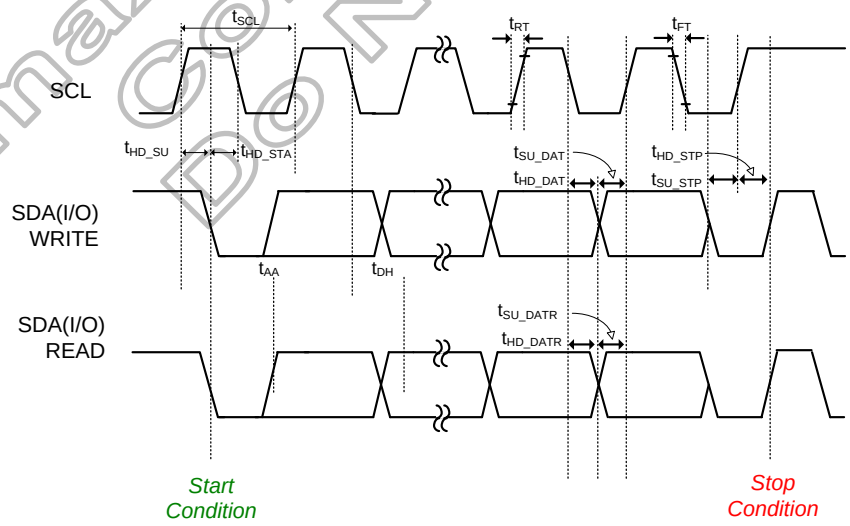


Figure 11.1: 2-Wire serial interface timing diagram

11.6. Parallel interface timing characteristics

Conditions: T_A = 25ºC, C_L = 15pF, F_{PLCKO} = 84.7MHz, IOVDD = 3.3V.

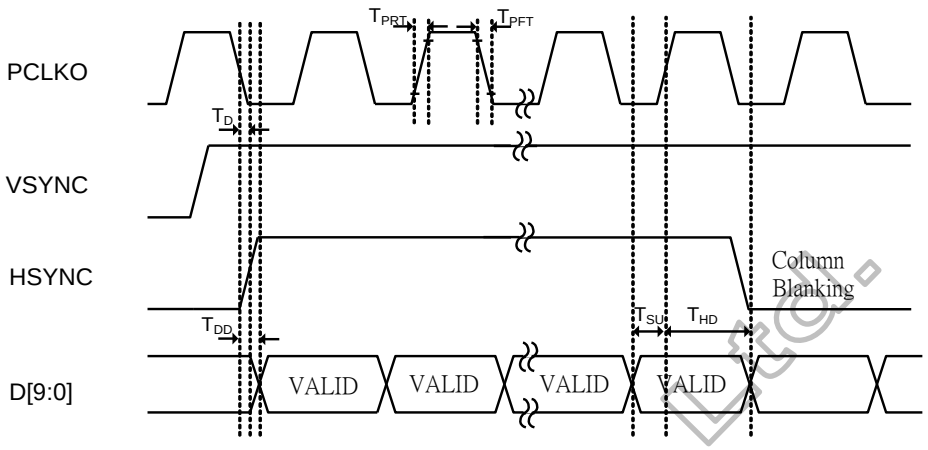


Figure 11.2: Parallel video interface timing diagram

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
PCLKO period	T_{PLCKO}	-	11.8	-	ns
PCLKO rise time	T_{PRT}	-	3	-	ns
PCLKO fall time	T_{PFT}	-	2.9	-	ns
PCLKO falling edge to HSYNC, VSYNC rising edge delay	T_D	-	0	-	ns
PCLKO falling edge to DATA transition delay	T_{DD}	-	0	-	ns
Data bus setup time	T_{SU}	-	5.9	-	ns
Data bus hold time	T_{HD}	-	5.9	-	ns

Table 11.6: Parallel video interface timing

12. Sensor Chief Ray Angle (CRA)

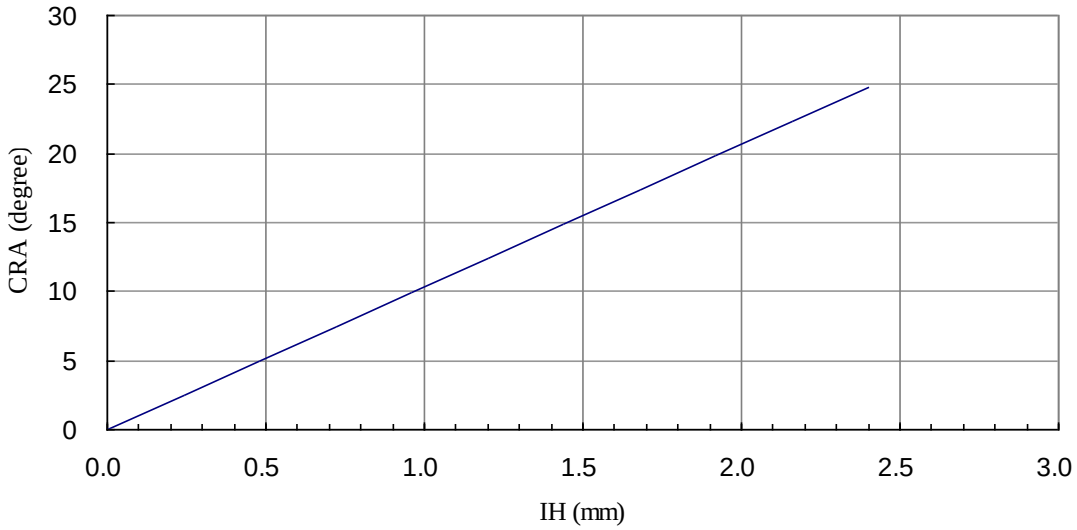


Figure 12.1: Lens CRA profile

Field (%)	Image Height (mm)	CRA (degree)
0.0	0.00	0.00
0.1	0.24	2.48
0.2	0.48	4.96
0.3	0.72	7.44
0.4	0.96	9.91
0.5	1.20	12.39
0.6	1.44	14.87
0.7	1.68	17.35
0.8	1.92	19.83
0.9	2.16	22.31
1.0	2.40	24.79

Table 12.1: CRA profile

13. Quantum Efficiency (QE)

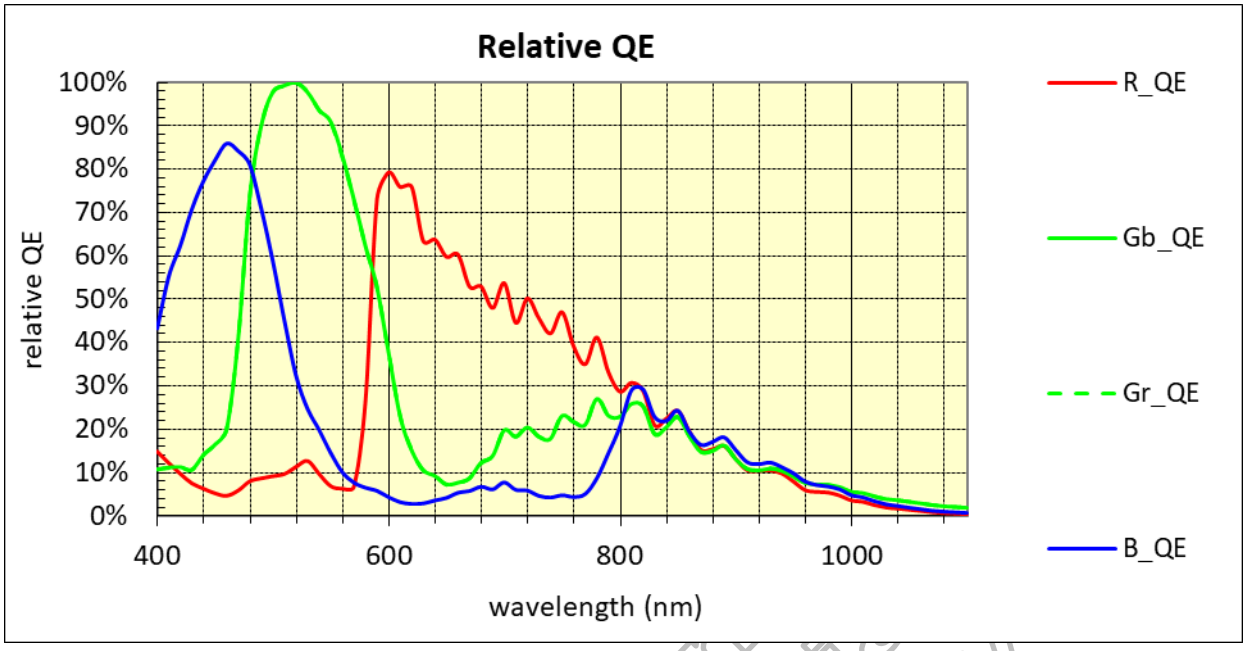


Figure 13.1: QE (Bayer)

14. Related Documents

Package Information and other Application Notes are available from Himax Imaging.